

## 2SK2978

Silicon N Channel MOS FET  
High Speed Power Switching

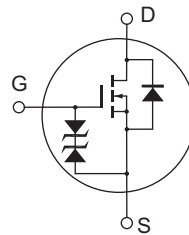
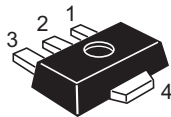
REJ03G1060-0500  
(Previous: ADE-208-659C)  
Rev.5.00  
Sep.07,2005

### Features

- Low on-resistance  
 $R_{DS(on)} = 0.09 \Omega$  typ. ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 1.5 \text{ A}$ )
- Low drive current
- High speed switching
- 2.5 V gate drive devices.

### Outline

RENESAS Package code: PLZZ0004CA-A  
(Package name: UPAK<sup>®</sup>)



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "ZY"

\*UPAK is a trademark of Renesas Technology Corp.

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	20	V
Gate to source voltage	$V_{GSS}$	±10	V
Drain current	$I_D$	2.5	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	5	A
Body-drain diode reverse drain current	$I_{DR}$	2.5	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	1	W
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Notes: 1.  $PW \leq 10\mu s$ , duty cycle  $\leq 1\%$ 

2. When using the alumina ceramic board (12.5 x 20 x 0.7 mm)

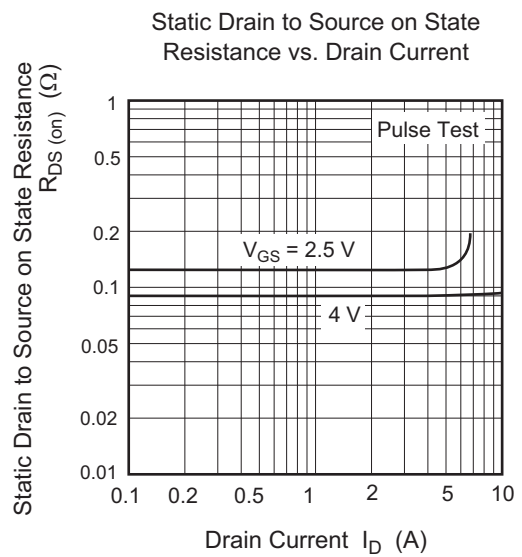
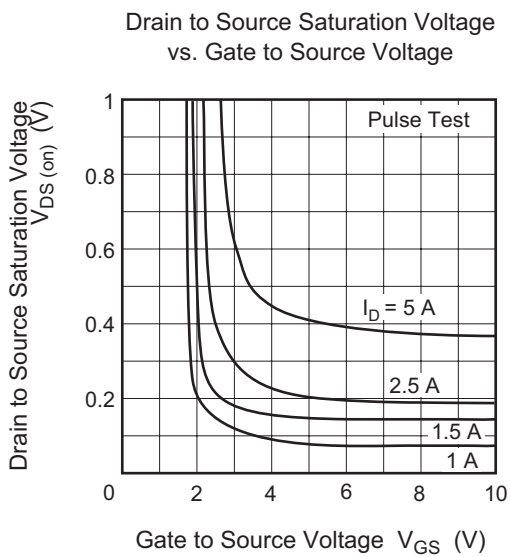
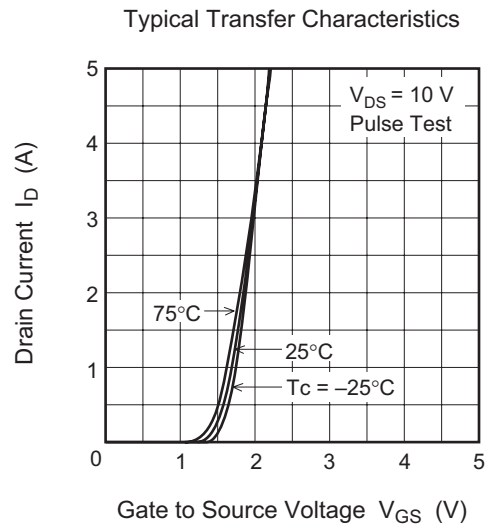
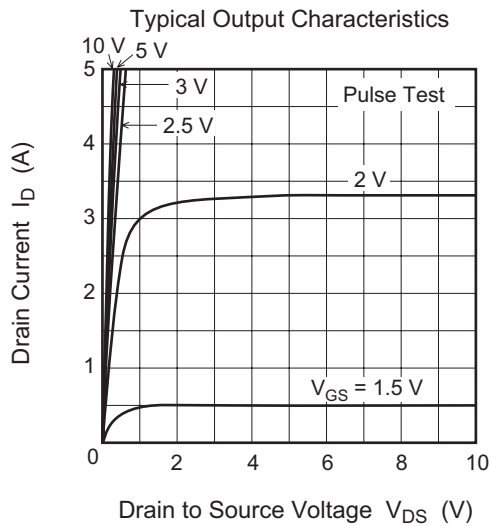
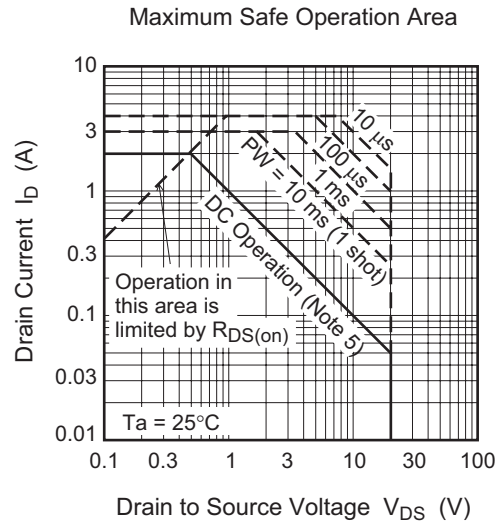
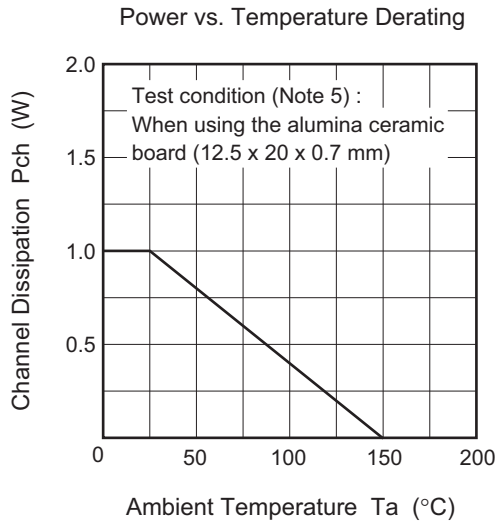
## Electrical Characteristics

(Ta = 25°C)

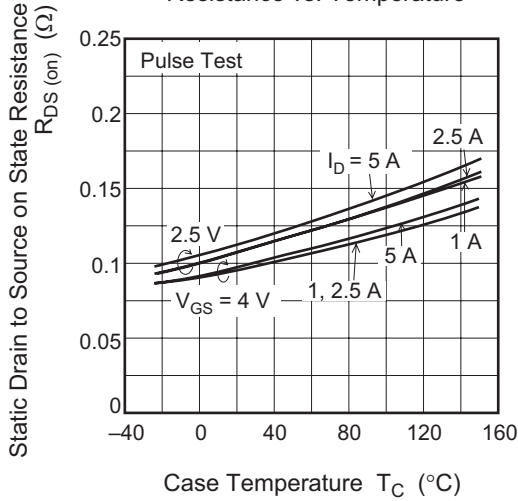
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 10\text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100\ \mu A$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu A$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	$\mu A$	$V_{GS} = \pm 8\text{ V}$ , $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.5	—	1.5	V	$I_D = 1\text{ mA}$ , $V_{DS} = 10\text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.09	0.12	$\Omega$	$I_D = 1.5\text{ A}$ , $V_{GS} = 4\text{ V}$ <sup>Note3</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.20	$\Omega$	$I_D = 1.5\text{ A}$ , $V_{GS} = 2.5\text{ V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	3.0	5.0	—	S	$I_D = 1.5\text{ A}$ , $V_{DS} = 10\text{ V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	260	—	pF	$V_{DS} = 10\text{ V}$ , $V_{GS} = 0$ , $f = 1\text{ MHz}$
Output capacitance	$C_{oss}$	—	150	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	75	—	pF	
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 4\text{ V}$ , $I_D = 1.5\text{ A}$ , $R_L = 6.67\ \Omega$
Rise time	$t_r$	—	70	—	ns	
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	
Fall time	$t_f$	—	70	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.9	—	V	$I_F = 2.5\text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	75	—	ns	$I_F = 2.5\text{ A}$ , $V_{GS} = 0$ $di_F/dt = 50\text{ A}/\mu s$

Note: 3. Pulse test

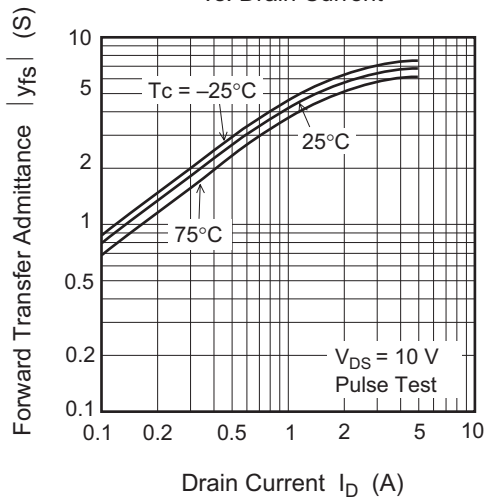
Main Characteristics



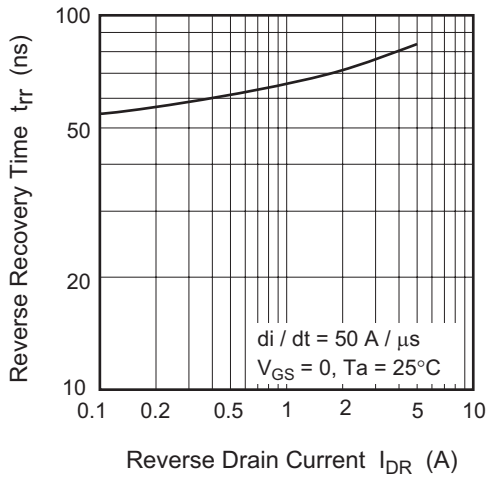
Static Drain to Source on State Resistance vs. Temperature



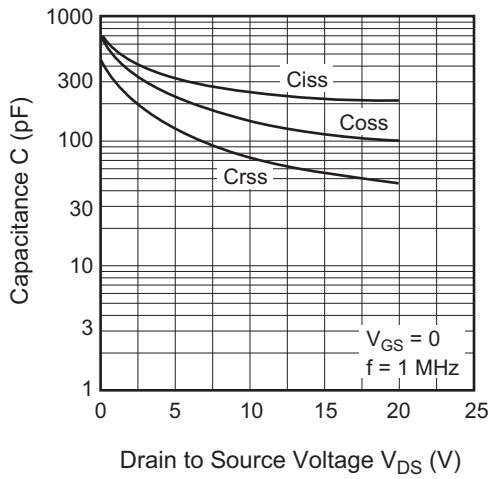
Forward Transfer Admittance vs. Drain Current



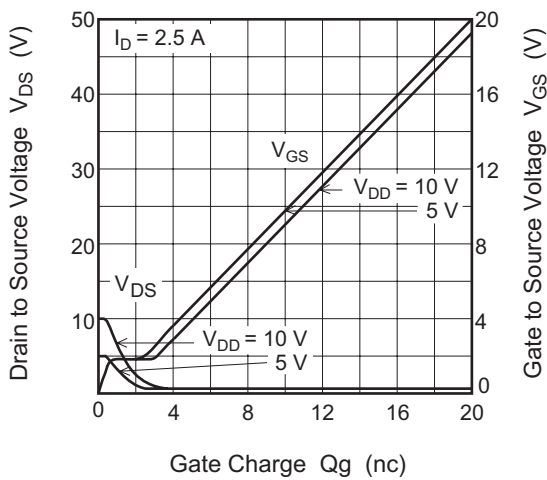
Body to Drain Diode Reverse Recovery Time



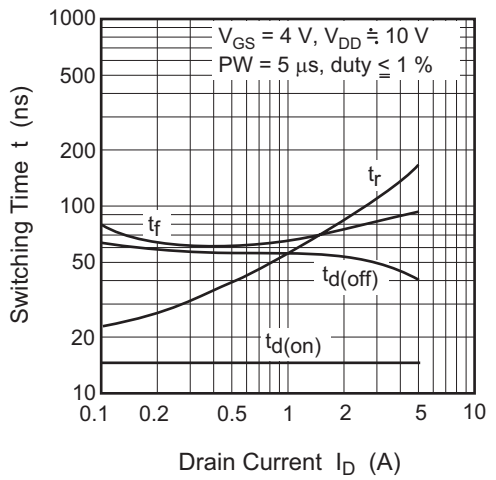
Typical Capacitance vs. Drain to Source Voltage



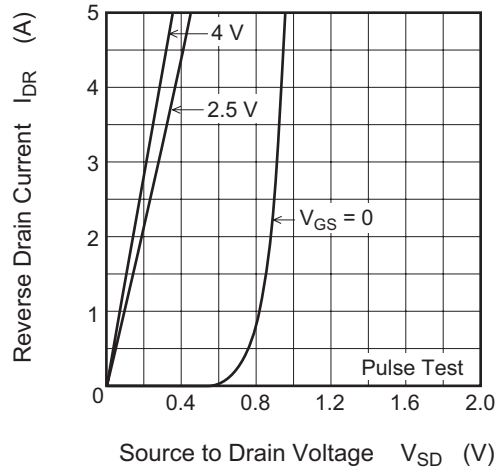
Dynamic Input Characteristics



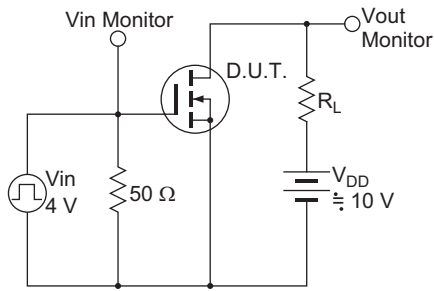
Switching Characteristics



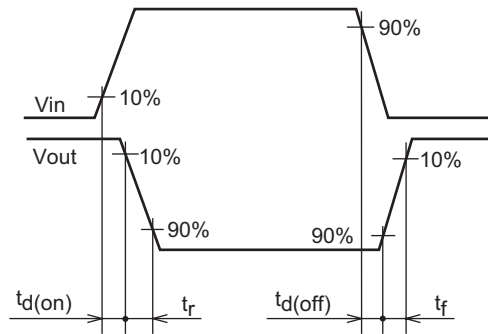
Reverse Drain Current vs. Source to Drain Voltage



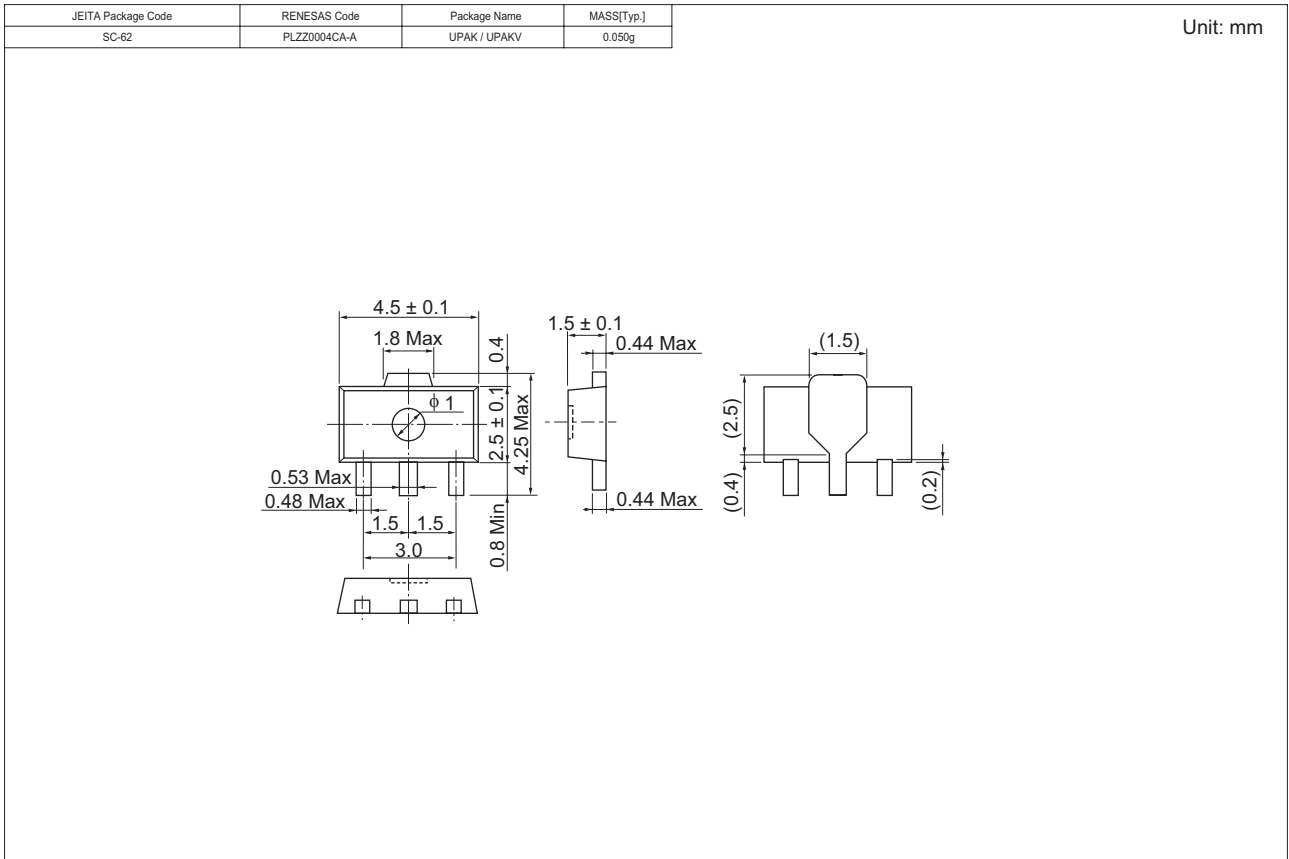
Switching Time Test Circuit



Waveform



## Package Dimensions



## Ordering Information

Part Name	Quantity	Shipping Container
2SK2978ZYTL-E	1000 pcs	Taping
2SK2978ZYTR-E	1000 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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