BURR - BROWN®

3554

Wideband, Fast-Settling OPERATIONAL AMPLIFIER

FEATURES

- SLEW RATE: 1000V/µs
- FAST SETTLING: 150ns, max (to ±0.05%)
- GAIN-BANDWIDTH PRODUCT, 1.7GHz
- FULL DIFFERENTIAL INPUT

APPLICATIONS

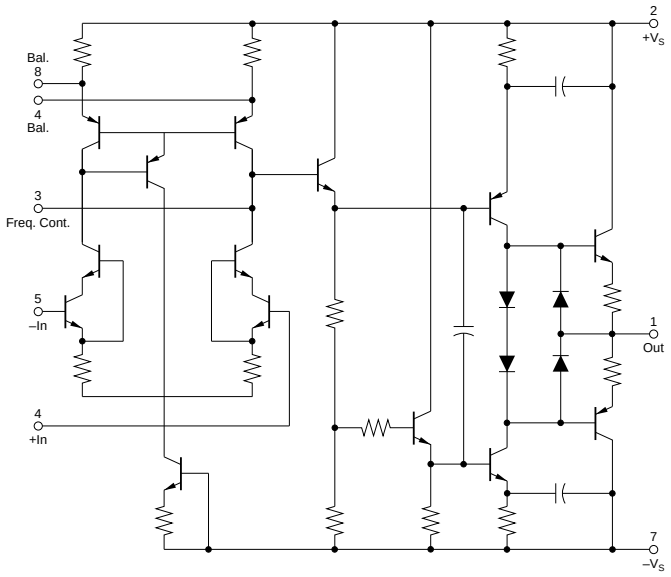
- PULSE AMPLIFIERS
- TEST EQUIPMENT
- WAVEFORM GENERATORS
- FAST D/A CONVERTERS

DESCRIPTION

The 3554 is a full differential input, wideband operational amplifier. It is designed specifically for the amplification or conditioning of wideband data signals and fast pulses. It features an unbeatable combination of gain-bandwidth product, settling time and slew rate. It uses hybrid construction. On the beryllia substrate are matched input FETs, thin-film resistors and high speed silicon dice. Active laser trimming and complete testing provide superior performance at a very moderate price.

The 3554 has a slew rate of 1000V/µs and will output ±10V and ±100mA. When used as a fast settling amplifier, the 3554 will settle to ±0.05% of the final value within 150ns. A single external compensation capacitor allows the user to optimize the bandwidth, slew rate or settling time in the particular application.

The 3554 is reliable and rugged, and addresses almost any application when speed and bandwidth are serious considerations. It is particularly a good choice for use in fast settling circuits, fast D/A converters, multiplexer buffers, comparators, waveform generators, integrators, and fast current amplifiers. It is available in several grades to allow selection of just the performance required.



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SPECIFICATIONS

ELECTRICAL

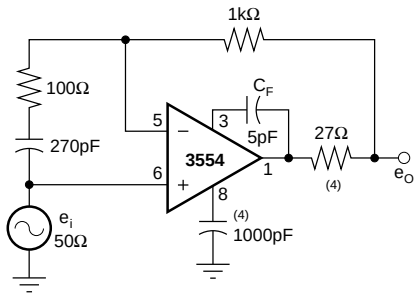
At T_{CASE} = +25°C and ±15VDC, unless otherwise noted.

PARAMETER	CONDITIONS	3554AM			3554BM			3554SM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC											
No Load		100	106		*	*		*	*		dB
Rated Load	R_L = 100Ω	90	96		*	*		*	*		dB
RATED OUTPUT											
Voltage	I_O = ±100mA	±10	±11		*	*		*	*		V
Current	V_O = ±10V	±100	±125		*	*		*	*		mA
Output Resistance, Open-Loop	f = 10MHz		20			*			*		Ω
DYNAMIC RESPONSE											
Bandwidth (0dB, small signal)	C_F = 0	70	90		*	*		*	*		MHz
Gain-bandwidth Product	C_F = 0, G = 10V/V	150	225		*	*		*	*		MHz
	C_F = 0, G = 100V/V	425	725		*	*		*	*		MHZ
	C_F = 0, G = 1000V/V	1000	1700		*	*		*	*		MHz
Full Power Bandwidth	C_F = 0, V_O = 20Vp-p, R_L = 100Ω	16	19		*	*		*	*		MHz
Slew Rate	C_F = 0, V_O = 20Vp-p, R_L = 100Ω	1000	1200		*	*		*	*		V/µs
Settling Time: to ±1%	A = 1		60			*			*		ns
to ±0.1%	A = 1		120			*			*		ns
to ±0.05%	A = 1		140	150		*	*		*	*	ns
to ±0.01%	A = 1		200	250		*	*		*	*	ns
INPUT OFFSET VOLTAGE											
Input Offset, T_A = 25°C			±0.5	±2		±0.2	±1		±0.2	±1	mV
vs Temp (T_A = –25°C to +85°C)			±20	±50		±8	±15				µV/°C
vs Temp (T_A = –55°C to +125°C)									±12	±25	µV/°C
vs Supply Voltage			±80	±300		*	*		*	*	µV/V
INPUT BIAS CURRENT											
Input Bias, 25°C		0	–10	–50	*	*	*	*	*	*	pA
vs Temp			(1)			*			*		
vs Supply Voltage			±1			*			*		pA/V
INPUT DIFFERENCE CURRENT											
Initial Difference, 25°C			±2	±10		*	*		*	*	pA
INPUT IMPEDANCE											
Differential			10^{11}|| 2			*			*		Ω || pF
Common-Mode			10^{11}|| 2			*			*		Ω || pF
INPUT NOISE											
Voltage, f_O = 1Hz	R_S = 100Ω		125			*			*		nV/√Hz
f_O = 10Hz	R_S = 100Ω		50			*			*		nV/√Hz
f_O = 100kHz	R_S = 100Ω		25			*			*		nV/√Hz
f_O = 1kHz	R_S = 100Ω		15			*			*		nV/√Hz
f_O = 10kHz	R_S = 100Ω		10			*			*		nV/√Hz
f_O = 100kHz	R_S = 100Ω		8			*			*		nV/√Hz
f_O = 1MHz	R_S = 100Ω		7			*			*		nV/√Hz
f_B = 0.3Hz to 10Hz	R_S = 100Ω		2			*			*		µVp-p
f_B = 10Hz to 1MHz	R_S = 100Ω		8			*			*		µVrms
Current, f_B = 0.3Hz to 10Hz	R_S = 100Ω		45			*			*		fAp-p
f_B = 10Hz to 1MHz	R_S = 100Ω		2			*			*		pArms
INPUT VOLTAGE RANGE											
Common-Mode Voltage Range	Linear Operation		±(|V_{CC}|–4)			*			*		V
Common-Mode Rejection	f = DC, V_{CM} = +7V, –10V	44	78		*	*		*	*		dB
Maximum Safe Input Voltage			±Supply			*			*		V
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated Performance		±5		±18	*		*	*		*	VDC
Current, Quiescent		±17	±35	±45	*	*	*	*	*	*	mA
TEMPERATURE RANGE											
Specification	Ambient Temperature	–25		+85	–25		+85	–55		+125	°C
Operating, Derated Performance	Ambient Temperature	–55		+125	–55		+125	–55		+125	°C
Storage	Ambient Temperature	–65		+150	–65		+150	–65		+150	°C
θ Junction-Case	Ambient Temperature		15			15			15		°C/W
θ Junction-Ambient	Ambient Tempterature		45			45			45		°C/W

* Specifications same as for 3554AM.

NOTE: (1) Doubles every +10°C.

AMPLIFIER CONNECTIONS



Gain = +1V/V(1)

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage	±18V
Input Voltage	$\pm V_S$
Output Short Circuit (to ground)	10s
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+165°C
Lead Temperature (soldering, 10s)	+300°C

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
3554AM	8-Pin Metal TO-3	–25°C to +85°C
3554BM	8-Pin Metal TO-3	–25°C to +85°C
3554SM	8-Pin Metal TO-3	–55°C to +125°C

PACKAGE INFORMATION(1)

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
3554AM	8-Pin Metal TO-3	030
3554BM	8-Pin Metal TO-3	030
3554SM	8-Pin Metal TO-3	030

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

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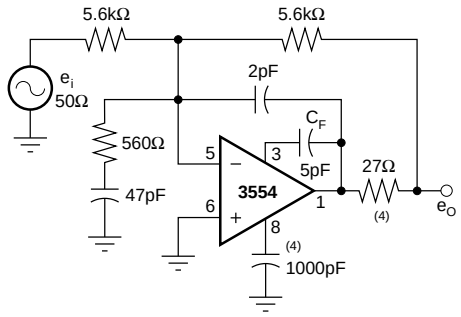
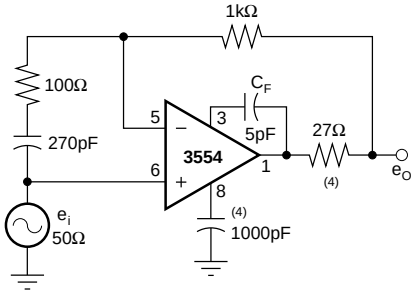
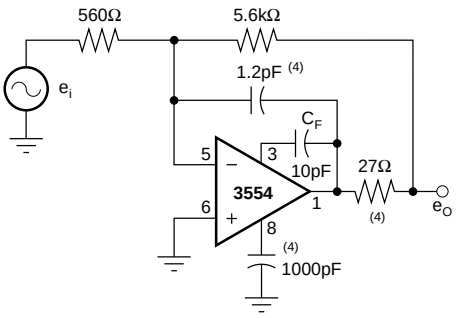
TYPICAL CIRCUITS



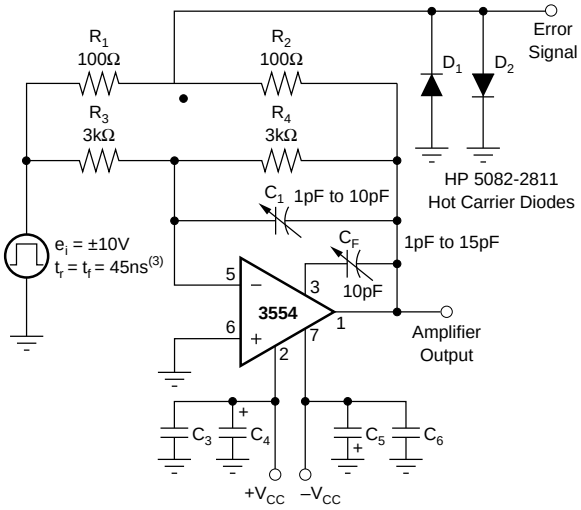
Gain = –1V/V (1)



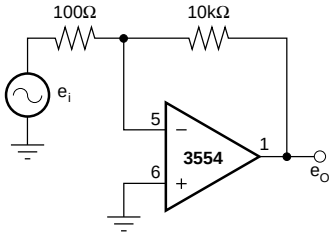
Gain = +1V/V(1)



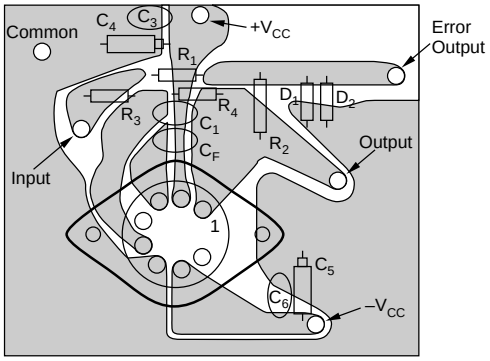
Gain = –10V/V(1)



Settling Time Test Circuit Schematic



Gain = +100V/V(2)



Settling Time Test Circuit Layout

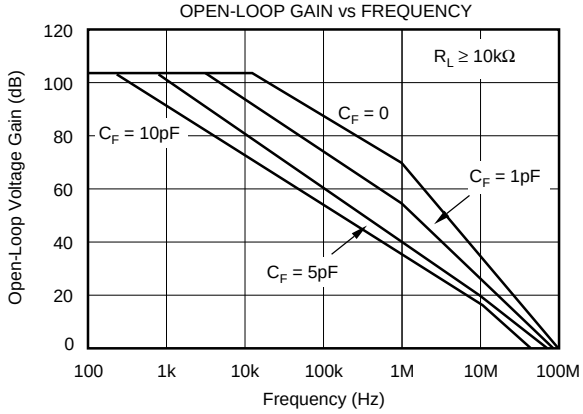
View from component side.
Shaded area is the pattern side conductor.

NOTES: (1) These circuits are optimized for driving large capacitive loads (to 470pF). (2) The 3554 is stable at gains of greater than 55 ($C_L \leq 100$pF) without any frequency compensation. (3) 45ns is optimum. Very fast rise times (10-20ns) may saturate the input stage causing less than optimum settling time performance. (4) Component may be eliminated when large capacitive loads are not being driven by the device.

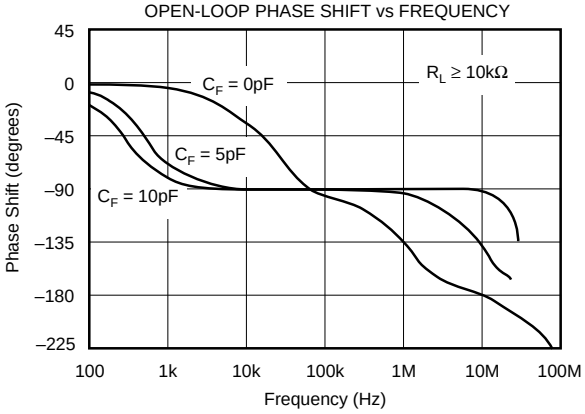
TYPICAL PERFORMANCE CURVES

At T_c = +25°C and ±15VDC, unless otherwise noted.

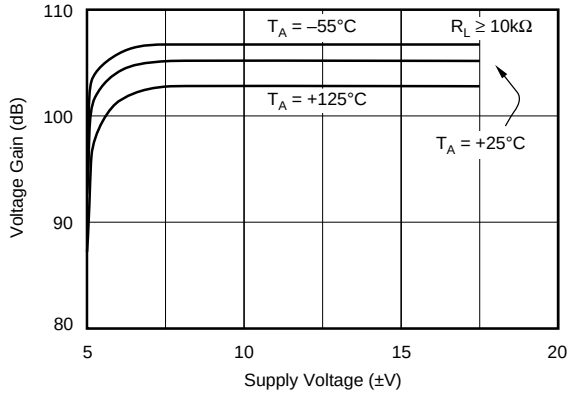
OPEN-LOOP GAIN vs FREQUENCY



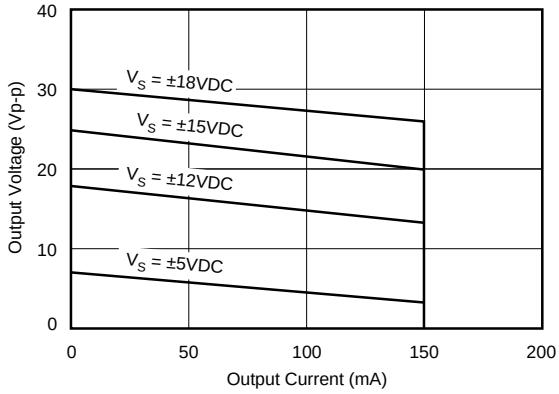
OPEN-LOOP PHASE SHIFT vs FREQUENCY



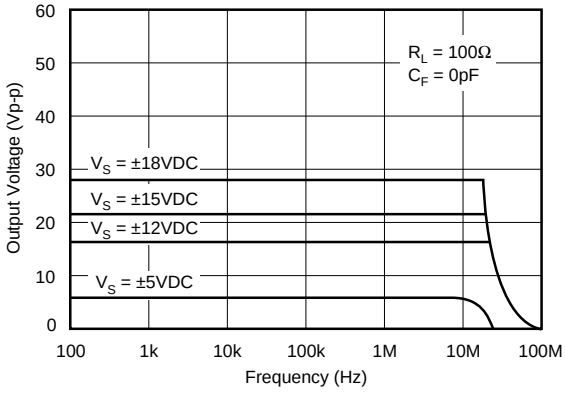
VOLTAGE GAIN vs SUPPLY VOLTAGE



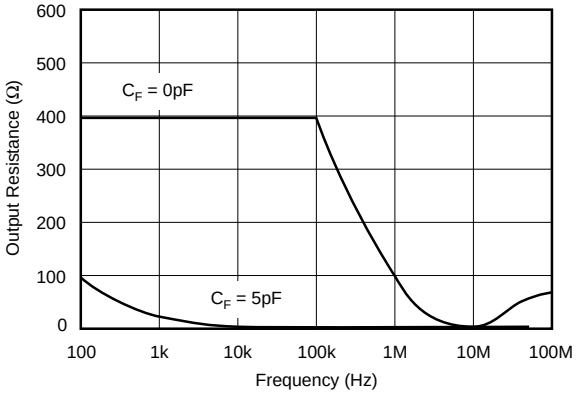
OUTPUT VOLTAGE vs OUTPUT CURRENT



OUTPUT VOLTAGE vs FREQUENCY



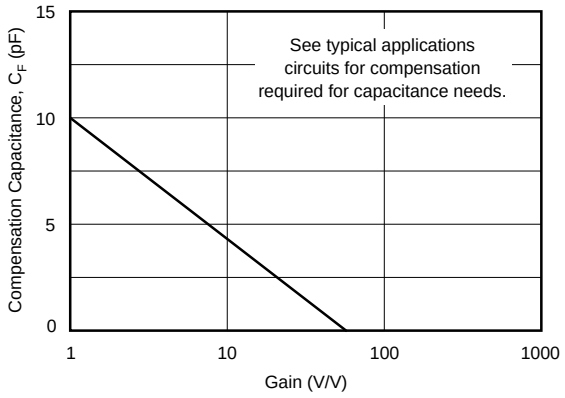
OPEN-LOOP OUTPUT RESISTANCE vs FREQUENCY



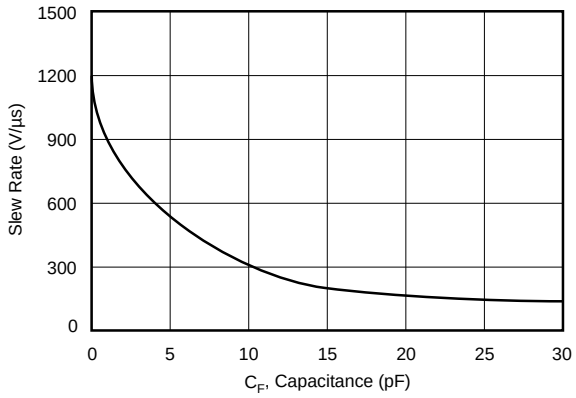
TYPICAL PERFORMANCE CURVES (CONT)

At T_c = +25°C and ±15VDC, unless otherwise noted.

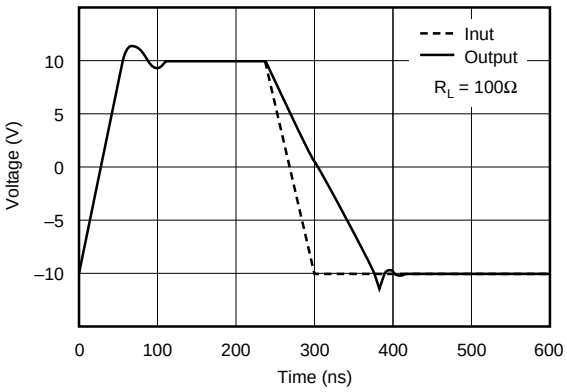
RECOMMENDED VALUES OF COMPENSATION CAPACITANCE vs CLOSED-LOOP GAIN



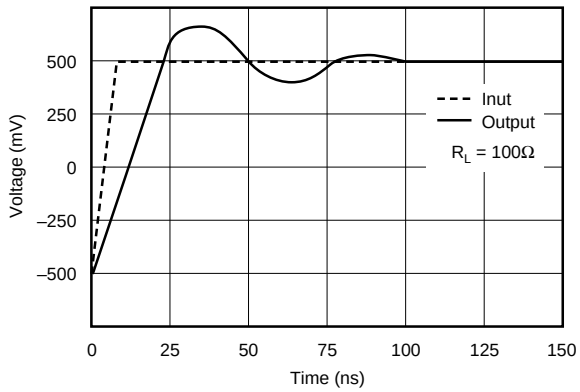
SLEW RATE



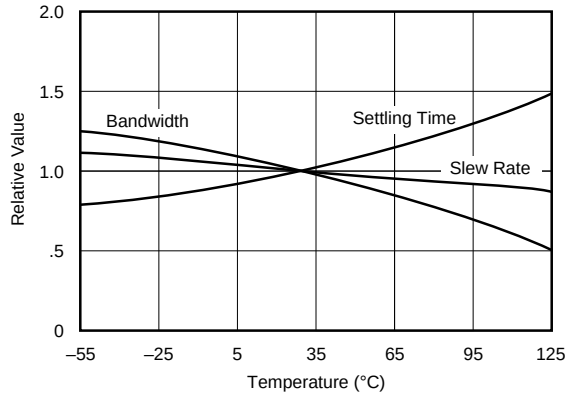
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



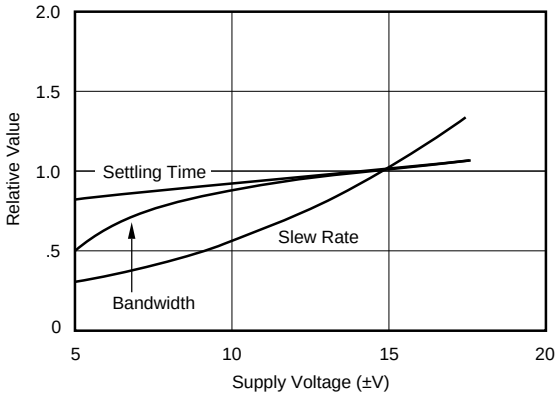
VOLTAGE FOLLOWER TRANSIENT RESPONSE



FREQUENCY CHARACTERISTICS



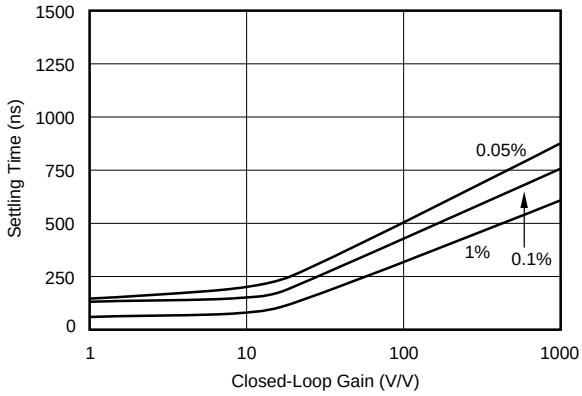
FREQUENCY CHARACTERISTICS



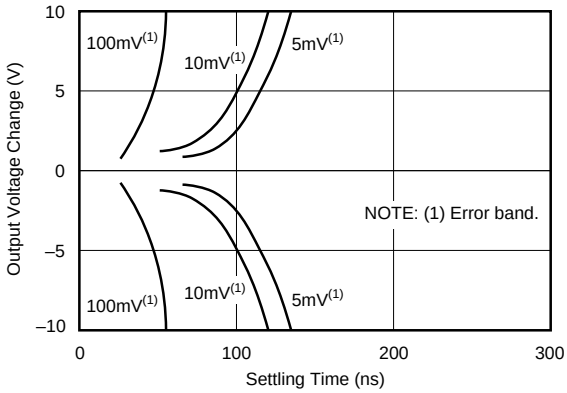
TYPICAL PERFORMANCE CURVES (CONT)

At T_C = +25°C and ±15VDC, unless otherwise noted.

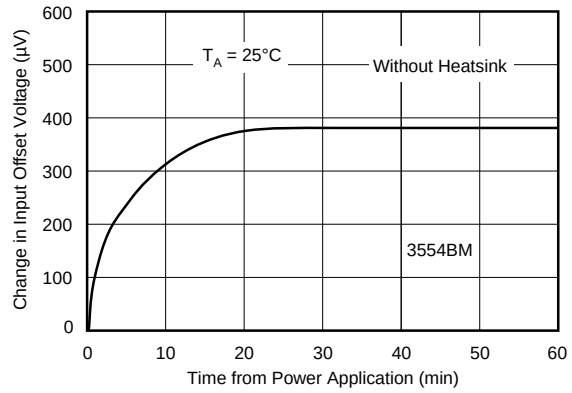
SETTLING TIME



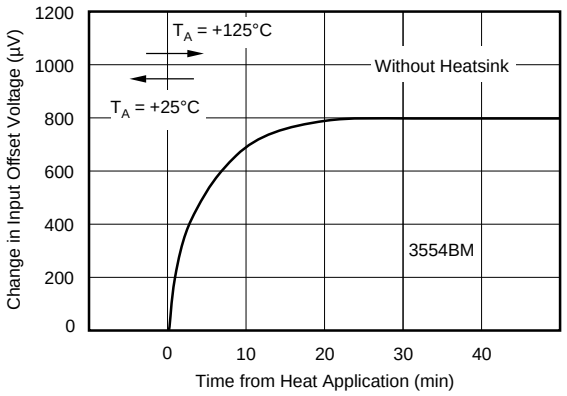
SETTLING TIME vs OUTPUT VOLTAGE CHANGE



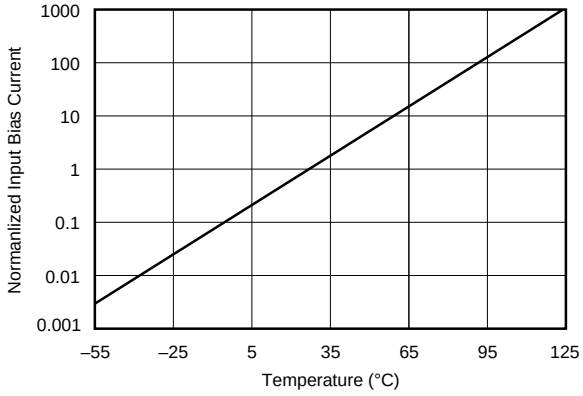
WARMUP DRIFT



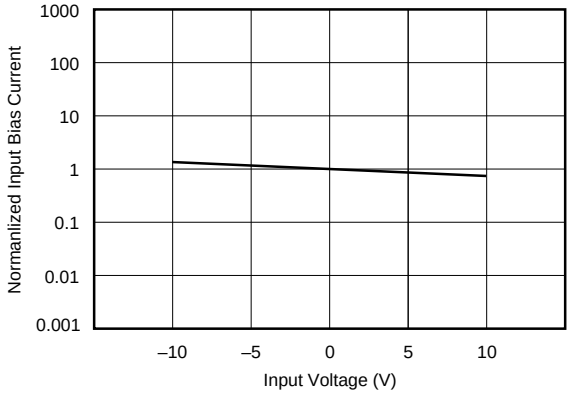
EFFECT OF THERMAL SHOCK ON OFFSET VOLTAGE



INPUT BIAS CURRENT



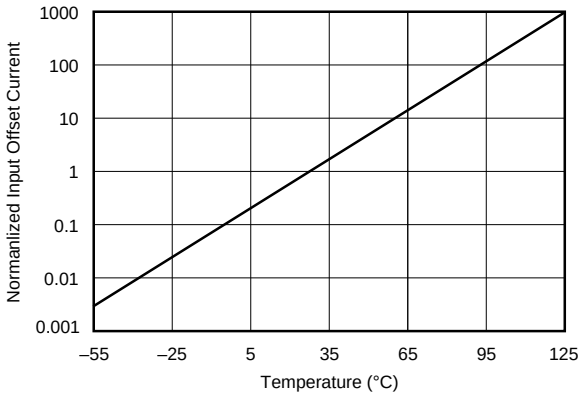
INPUT BIAS CURRENT



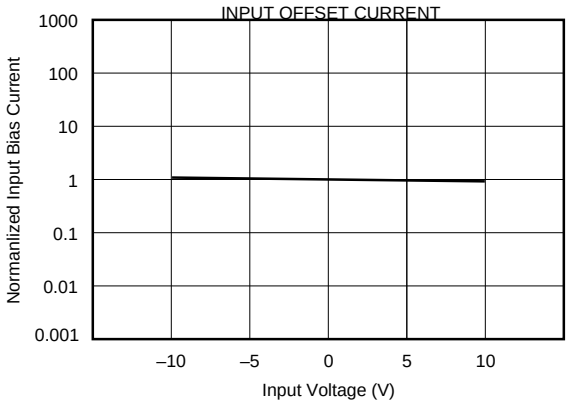
TYPICAL PERFORMANCE CURVES (CONT)

At T_c = +25°C and ±15VDC, unless otherwise noted.

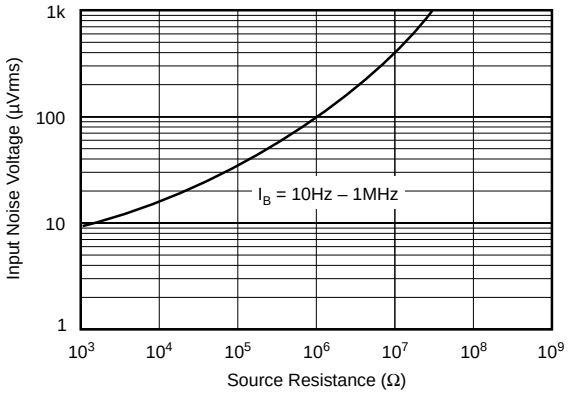
INPUT OFFSET CURRENT



INPUT OFFSET CURRENT

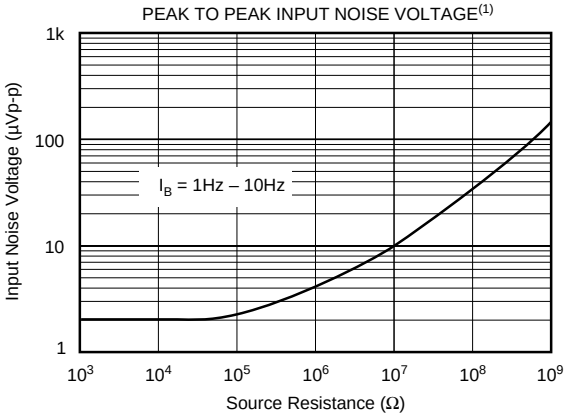


RMS INPUT NOISE VOLTAGE(1)



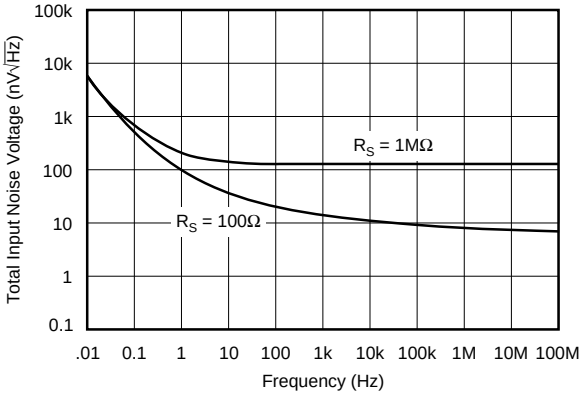
NOTE: (1) Includes contribution from source resistance.

PEAK TO PEAK INPUT NOISE VOLTAGE(1)



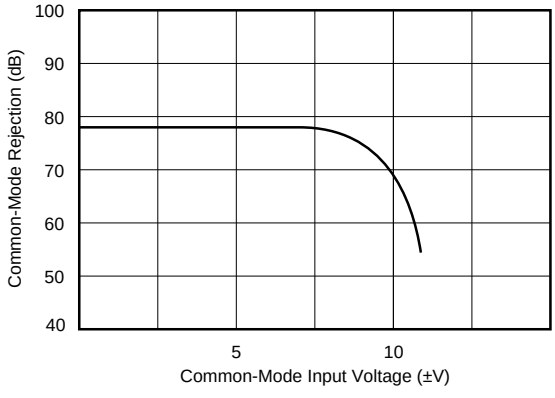
NOTE: (1) Includes contribution from source resistance.

TOTAL INPUT NOISE VOLTAGE(1)



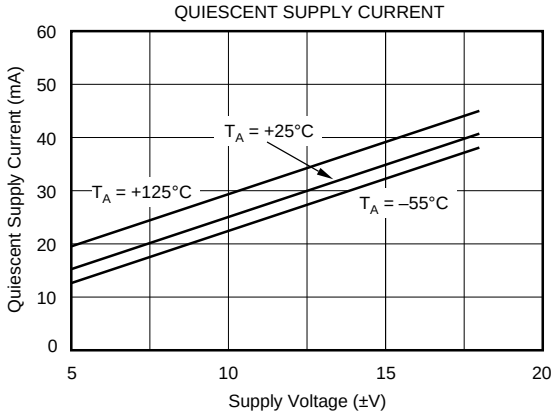
NOTE: (1) Includes contribution from source resistance.

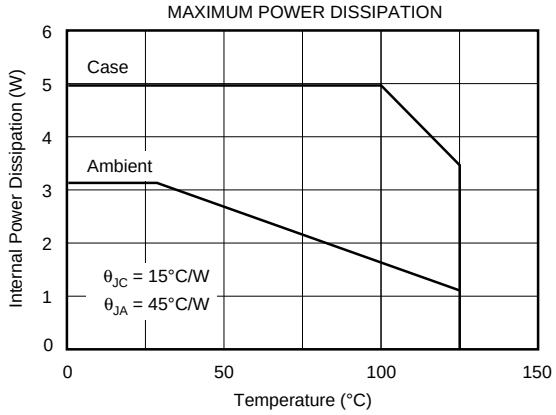
COMMON-MODE REJECTION



TYPICAL PERFORMANCE CURVES (CONT)

At T_C = +25°C and ±15VDC, unless otherwise noted.





APPLICATIONS INFORMATION

WIRING PRECAUTIONS

The 3554 is a wideband, high frequency operational amplifier that has a gain-bandwidth product exceeding 1GHz. The full performance capability of this amplifier will be realized by observing a few wiring precautions and high frequency techniques.

Of all the wiring precautions, grounding is the most important and is described in an individual section. The mechanical circuit layout also is very important. All circuit element leads should be as short as possible. All printed circuit board conductors should be wide to provide low resistance, low inductance connections and should be as short as possible. In general, the entire physical circuit should be as small as practical. Stray capacitances should be minimized especially at high impedance nodes such as the input terminals of the amplifier. Pin 5, the inverting input, is especially sensitive and all associated connections must be short. Stray signal coupling from the output to the input or to pin 8 should be minimized. A recommended printed circuit board layout is shown with the "Typical Circuits." It may also be used for test purposes as described below.

When designing high frequency circuits low resistor values should be used; resistor values less than 5.6kΩ are recommended. This practice will give the best circuit performance as the time constants formed with the circuit capacitances will not limit the performance of the amplifier.

GROUNDING

As with all high frequency circuits, a ground plane and good grounding techniques should be used. The ground plane should connect all areas of the pattern side of the printed circuit board that are not otherwise used. The ground plane provides a low resistance, low inductance common return path for all signal and power returns. The ground plane also reduces stray signal pick up. An example of an adequate ground plane and good high frequency techniques is the Settling Time Test Circuit Layout shown with the "Typical Circuits."

Each power supply lead should be bypassed to ground as near as possible to the amplifier pins. A combination of a 1µF tantalum capacitor in parallel with a 470pF ceramic capacitor is a suitable bypass.

In inverting applications it is recommended that pin 6, the noninverting input, be grounded rather than being connected to a bias current compensating resistor. This assures a good signal ground at the noninverting input. A slight offset error will result, however, because the resistor values normally used in high frequency circuits are small and the bias current is small, the offset error will be minimal.

If point-to-point wiring is used or a ground plane is not, single point grounding should be used. The input signal return, the load signal return, and the power supply common should all be connected at the same physical point. This will eliminate any common current paths or ground loops which could cause signal modulation or unwanted feedback.

It is recommended that the case of the 3554 not be grounded during use (it may, if desired). A grounded case will add a slight capacitance to each pin. To an already functional circuit, grounding the case will probably require slight compensation readjustment and the compensation capacitor values will be slightly different from those recommended in the typical performance curves. There is no internal connection to the case.

Proper grounding is the single most important aspect of high frequency circuitry.

GUARDING

The input terminals of the 3554 may be surrounded by a guard ring to divert leakage currents from the input terminals. This technique is particularly important in low bias current and high input impedance applications. The guard, a conductive path that completely surrounds the two amplifier inputs, should be connected to a low impedance point which is at the input signal potential. It blocks unwanted printed circuit board leakage currents from reaching the input terminals. The guard will also reduce stray signal coupling to the input.

In high frequency applications, guarding may not be desirable as it increases the input capacitance and can degrade performance. The effects of input capacitance, however, can be compensated by a small capacitor placed across the feedback resistor. This is described further in the following section.

COMPENSATION

The 3554 uses external frequency compensation so that the user may optimize the bandwidth or slew rate or settling time for his particular application. Several typical performance curves are provided to aid in the selection of the correct compensation capacitance value. In addition, several typical circuits show recommended compensation in different applications.

The primary compensation capacitor, C_F, is connected between pins 1 and 3. As the performance curves show, larger closed-loop gain configurations require less capacitance and an improved gain-bandwidth product will be realized. Note that no compensation capacitor is required for closed-loop gains above 55V/V and when the load capacitance is less than 100pF.

When driving large capacitive loads, 470pF and greater, an additional capacitor, C_8, is connected between pin 8 and ground. This capacitor is typically 1000pF. It is particularly necessary in low closed loop voltage gain configurations. The value may be varied to optimize performance and will depend upon the load capacitance value. In addition, the performance may be optimized by connecting a small resistance in series with the output and a small capacitor from pin 1 to 5. See the "Typical Circuits" for the XGain = –10V/V circuit.

The flat high frequency response of the 3554 may be preserved and any high frequency peaking avoided by connecting a small capacitor in parallel with the feedback resistor. This capacitor will compensate for the closed-loop, high frequency, transfer function zero that results from the time constant formed by the input capacitance of the amplifier, typically 2pF, and the input and feedback resistors. Using small resistor values will keep the break frequency of this zero sufficiently high, avoiding peaking and preserving the phase margin. Resistor values less than 5.6kΩ are recommended. The selected compensation capacitor may be a trimmer, a fixed capacitor, or a planned PC board capacitance. The capacitance value is strongly dependent on circuit layout and closed-loop gain. It will typically be 2pF for a clean layout using low resistances (1kΩ) and up to 10pF for circuits using larger resistances.

SETTLING TIME

Settling time is a complete dynamic measure of the 3554's total performance. It includes the slew rate time (a large signal dynamic parameter) and the time to accurately reach the final value (a small signal parameter that is a function of bandwidth and open loop-gain). The settling time may be optimized for the particular application by selection of the closed-loop gain and the compensation capacitance. The best settling time is observed in low closed-loop gain circuits. A performance curve shows the settling time to three different error bands.

Settling time is defined as the total time required from the signal input step for the output to settle to within the specified error band around the final value. This error band is expressed as a percentage of the magnitude of the output transition.

SLEW RATE

Slew rate is primarily an output, large signal parameter. It has virtually no dependence upon the closed-loop gain or the bandwidth. It is dependent upon compensation. Decreasing the compensation capacitor value will increase the available slew rate as shown in the performance curve. Stray capacitances may appear to the amplifier as compensation. To avoid limiting the slew rate performance, stray capacitances should be minimized.

CAPACITIVE LOADS

The 3554 will drive large capacitive loads (up to 1000pF) when properly compensated. See the section on "Compensation." The effect of a capacitive load is to decrease the phase margin of the amplifier. With compensation the amplifier will provide stable operation even with large capacitive loads.

The 3554 is particularly well suited for driving 50Ω loads connected via coaxial cables due to its ±100mA output drive capability. The capacitance of the coaxial cable, 29pF/foot of length for RG-58, does not load the amplifier when the coaxial cable or transmission line is terminated in the characteristic impedance of the transmission line.

OFFSET VOLTAGE ADJUSTMENT

The offset voltage of the 3554 may be adjusted to zero by connecting a 20kΩ linear potentiometer between pins 4 and 8 with the wiper connected to the positive supply. A small, noninductive potentiometer is recommended. The leads connecting the potentiometer to pins 4 and 8 should be extremely short to avoid stray capacitance and stray signal pickup. Stray coupling from the output, pin 1, to pin 4 (negative feedback) or to pin 8 (positive feedback) should be avoided or oscillation may occur.

The potentiometer is optional and may be omitted when the guaranteed offset voltage is considered sufficiently low for the particular application.

For each microvolt of offset voltage adjusted, the offset voltage temperature drift will change by ±0.004μV/°C.

HEAT SINKING

The 3554 does not require a heat sink for operation in most environments. The use of a heat sink, however, will reduce the internal thermal rise and will result in cooler operating temperatures. At extreme temperature and under full load conditions a heat sink will be necessary as indicated in the "Maximum Power Dissipation" curve. A heat sink with 8 holes for the 8 amplifier pins should be used. Burr-Brown has heat sinks available in three sizes –3°C/W, 4.2°C/W and 12°C/W. A separate product data sheet is available upon request.

When heat sinking the 3554, it is recommended that the heat sink be connected to the amplifier case and the combination not connected to the ground plane. For a single-sided printed circuit board, the heat sink may be mounted between the 3554 and the nonconductive side of the PC board, and insulating washers, etc., will not be required. The addition of a heat sink to an already functional circuit will probably require slight compensation readjustment for optimum performance due to the change in stray capacitances. The added stray capacitance from the heat sink to each pin will depend on the thickness and type of heat sink used.

SHORT CIRCUIT PROTECTION

The 3554 is short circuit protected for continuous output shorts to common. Output shorts to either supply will destroy the device, even for momentary connections. Output shorts to other potential sources are not recommended as they may cause permanent damage.

TESTING

The 3554 may be tested in conventional operational amplifier test circuits; however, to realize the full performance capabilities of the 3554, the test fixture must not limit the full dynamic performance capability of the amplifier. High frequency techniques must be employed. The most critical dynamic test is for settling time. The 3554 Settling Time Test Circuit Schematic and a test circuit layout is shown with the "Typical Circuits." The input pulse generator must have a flat topped, fast settling pulse to measure the true settling time of the amplifier. The layout exemplifies the high frequency considerations that must be observed. The layout also may be used as a guide for other test circuits. Good grounding, truly square drive signals, minimum stray coupling and small physical size are important.

Every 3554 is thoroughly tested prior to shipment assuring the user that all parameters equal or exceed their specifications.

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