

HD74HC74

Dual D-type Flip-Flops (with Preset and Clear)

REJ03D0549-0300 Rev.3.00 Oct 27, 2008

Description

The flip-flop has independent data, preset, clear, and clock inputs and Q and \overline{Q} outputs. The logic level present at the data input is transferred to the output during the positive going transition to the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

Features

- High Speed Operation: t_{pd} (Clock to Q or \overline{Q}) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max (Ta = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC74P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	Ρ	_
HD74HC74FPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74HC74RPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)
HD74HC74TELL	TSSOP-14 pin	PTSP0014JA-B (TTP-14DV)	т	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

	Inp	Outputs					
Preset	Clear	Clock	Data	Q	Q		
L	Н	Х	Х	Н	L		
Н	L	Х	Х	L	Н		
L	L	Х	Х	H ^{*1}	H ^{*1}		
Н	Н		Н	Н	L		
Н	Н		L	L	Н		
Н	Н	L	Х	No change			
Н	Н	Н	Х	No change			
Н	Н		Х	No change			

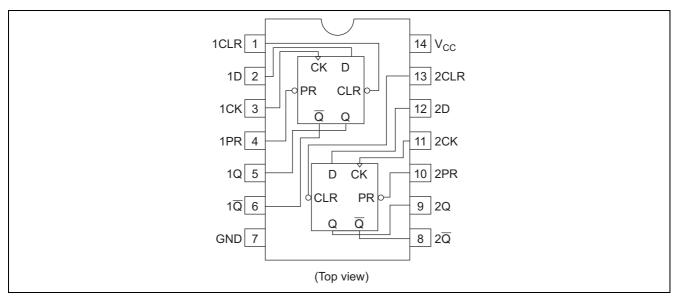
H: High level

L: Low level

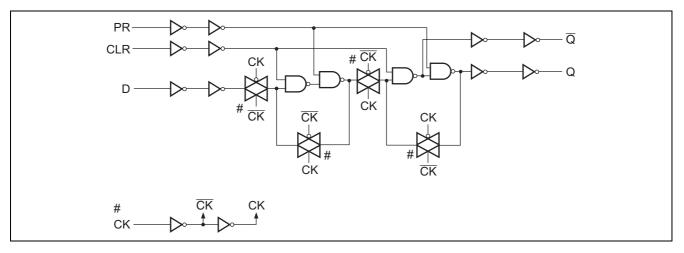
X: Irrelevant

Note: 1. Q and \overline{Q} will remain High as long as Preset and Clear are Low, but Q and \overline{Q} are unpredictable, if Preset and Clear go High simultaneously.

Pin Arrangement



Logic Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
Input / Output voltage	Vin, Vout	-0.5 to V _{CC} +0.5	V
Input / Output diode current	Iik, Iok	±20	mA
Output current	lo	±25	mA
V _{CC} , GND current	I _{CC} or I _{GND}	±50	mA
Power dissipation	PT	500	mW
Storage temperature	Tstg	-65 to +150	۵°

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Item	Symbol	Ratings	Unit	Conditions	
Supply voltage	V _{CC}	2 to 6	V		
Input / Output voltage	V _{IN} , V _{OUT}	0 to V _{CC}	V		
Operating temperature	Та	-40 to 85	°C		
		0 to 1000		$V_{CC} = 2.0 V$	
nput rise / fall time ^{*1}	t _r , t _f	0 to 500	ns	$V_{CC} = 4.5 V$	
		0 to 400	1	$V_{CC} = 6.0 V$	

Note: 1. This item guarantees maximum limit when one input switches. Waveform: Refer to test circuit of switching characteristics.

ltem	Symbol	v 00	Т	a = 25°	С	Ta = -40	to+85°C	11mi4	Test Conditions	
		V _{cc} (V)	Min	Тур	Max	Min	Max	Unit		
		2.0	1.5		—	1.5				
	VIH	4.5	3.15			3.15		V		
Input voltage		6.0	4.2	_	—	4.2				
input voltage		2.0	—	_	0.5		0.5			
	VIL	4.5	—	_	1.35	—	1.35	V		
		6.0	—		1.8		1.8			
	V _{он}	2.0	1.9	2.0	—	1.9			Vin = V _{IH} or V _{IL} $\frac{I_{OH} = -20 \ \mu A}{I_{OH} = -4 \ m A}$ $\frac{I_{OH} = -4 \ m A}{I_{OH} = -5.2 \ m A}$	
		4.5	4.4	4.5	—	4.4				$I_{OH} = -20 \ \mu A$
		6.0	5.9	6.0	—	5.9	—	V		
		4.5	4.18	_	—	4.13	—			$I_{OH} = -4 \text{ mA}$
Output voltage		6.0	5.68	_	—	5.63	—			$I_{OH} = -5.2 \text{ mA}$
Output voltage		2.0	—	0.0	0.1		0.1			
		4.5	—	0.0	0.1		0.1			I _{OL} = 20 μA
	V _{OL}	6.0	—	0.0	0.1		0.1	V	Vin = V _{IH} or V _{IL} $I_{OL} = 4 \text{ mA}$	
		4.5	—		0.26		0.33			$I_{OL} = 4 \text{ mA}$
		6.0	—		0.26		0.33			$I_{OL} = 5.2 \text{ mA}$
Input current	lin	6.0	_	_	±0.1		±1.0	μA	$Vin = V_{CC} \text{ or } GN$	ID
Quiescent supply current	I _{CC}	6.0			2.0		20	μΑ	$Vin = V_{CC} \text{ or } GN$	ID, Iout = 0 μ A

Electrical Characteristics

Switching Characteristics

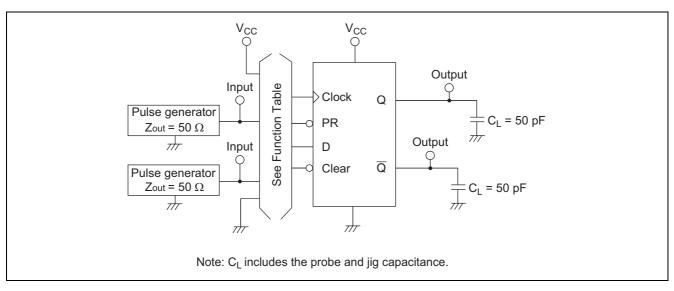
 $(C_L = 50 \text{ pF}, \text{ Input } t_r = t_f = 6 \text{ ns})$

ltem	Symbol	V _{cc} (V)	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
	Symbol	VCC (V)	Min	Тур	Max	Min	Max	Unit	Test conditions
		2.0	l		5	_	4		
Maximum clock frequency	f _{max}	4.5	l	35	25	_	20	MHz	
licquency		6.0	l		29	_	24		
	t _{PLH} , t _{PHL}	2.0		_	160	_	200	ns	
		4.5		14	32	_	40		Clock to Q or \overline{Q}
Propagation delay		6.0	_	_	27	—	34		
time		2.0	_	_	160	—	200	ns	Preset or Clear to Q or \overline{Q}
		4.5	_	13	32	—	40		
		6.0	_	_	27	—	34		
		2.0	100	_		125	—	ns	Data to Clock
Setup time	t _{su}	4.5	20	1		25	—		
		6.0	17	_	_	21	—		

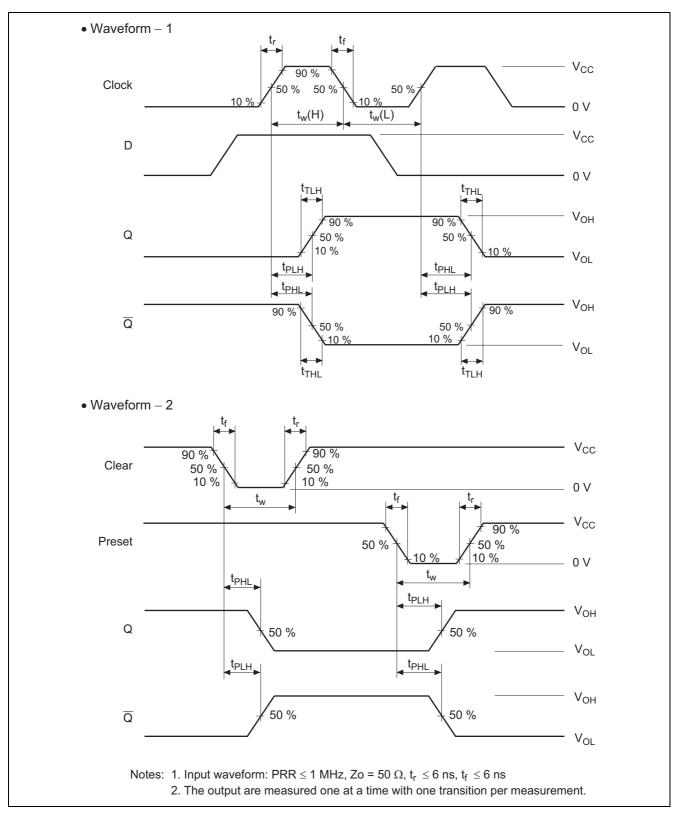
Switching Characteristics

									$(C_L = 50 \text{ pF}, \text{ Input } t_r = t_f = 6 \text{ ns})$
ltem	Symbol	V 00	Ta = 25°C Ta = -40 to +85°C			to +85°C	Unit	Test Conditions	
	Symbol	V _{cc} (V)	Min	Тур	Max	Min	Max	Unit	Test Conditions
		2.0	5	_		5	—		
Hold time	t _h	4.5	5	0		5	—	ns	Clock to Data
		6.0	5	-5	_	5	—		
	t _{rem}	2.0	25	_	_	31	—	ns	Preset, Clear to Clock
Removal time		4.5	5	_	—	6	—		
		6.0	4	_	—	5	—		
		2.0	80	_	—	100	—		Clock, Preset, Clear
Pulse width	t _w	4.5	16	8	—	20	—	ns	
		6.0	14	_		17	—		
Output rise/fall time		2.0	l	_	75	_	95		
	t_{TLH}, t_{THL}	4.5		5	15	_	19	ns	
		6.0		_	13	_	16		
Input capacitance	Cin	_	—	5	10	_	10	pF	

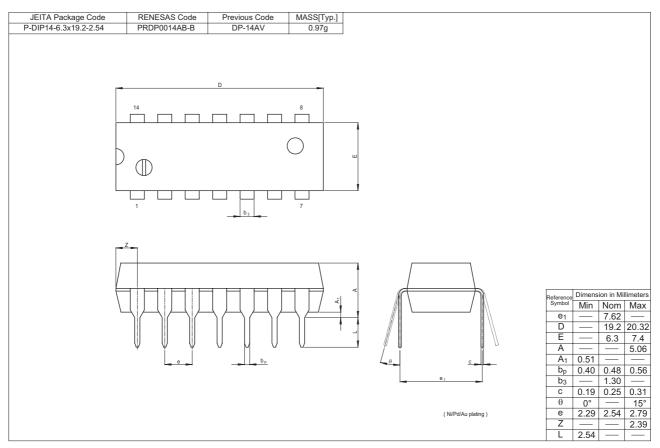
Test Circuit

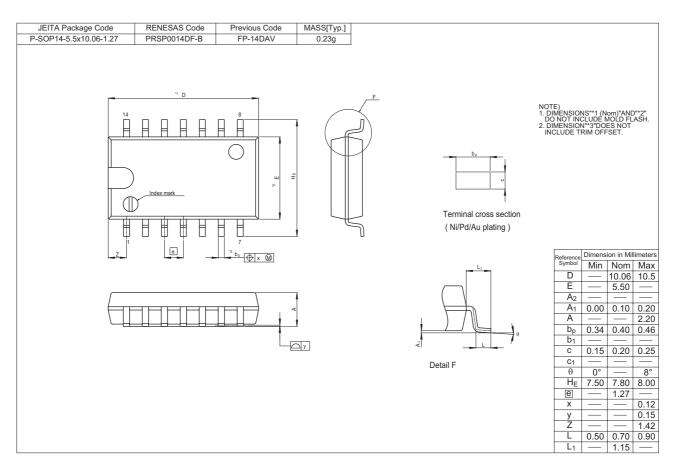


Waveforms



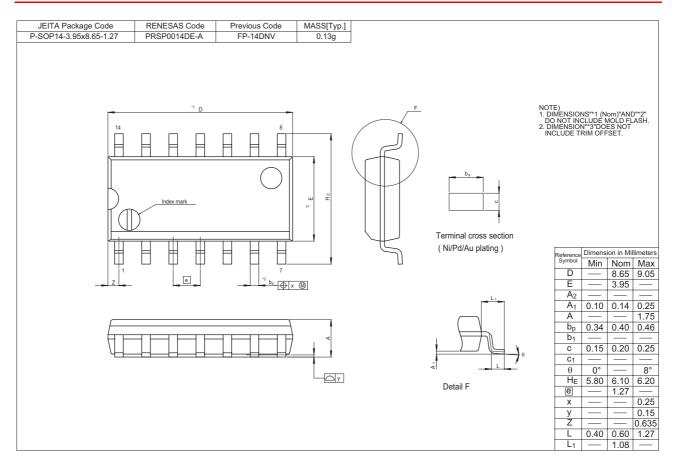
Package Dimensions

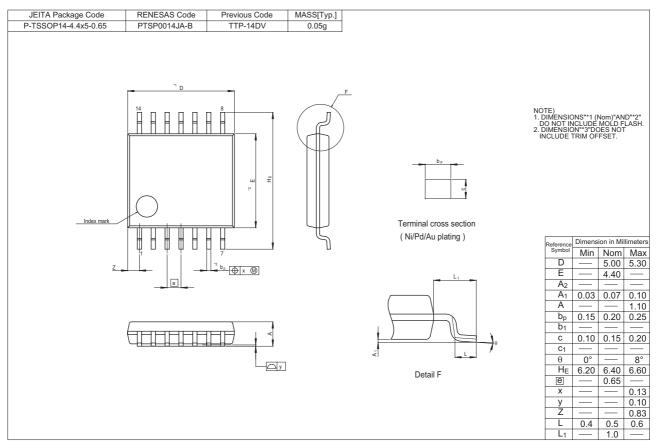




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