M66313FP

32-Bit LED Driver with Shift Register and Latch

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Description

The M66313FP is a semiconductor integrated circuit for LED array driver with 32-bit serial-input, parallel-output shift register, equipped with direct set input and output latches.

The M66313FP guarantees sufficient 24 mA output current to drive anode common LED, allowing 32-bit simultaneous and continuous current output.

The parallel outputs are open-drain outputs.

The M66313FP employs CMOS technology, allowing considerable reduction of power dissipation, compared to previous BIPOLAR or Bi-CMOS products.

In addition, the pin configuration is suitable for easy wiring on the printed circuit board.

Features

- High output current.
  All parallel output I_{OL} = +24 mA, LEDs can be turned on simultaneously.
- Low power dissipation : 200 μW/package (max)
  (V_{CC} = 5 V, Ta = 25°C, quiescent state)
- High noise margin
  Employment of Schmitt–trigger circuit on all inputs allows application with long wiring.
- Direct set input ($\overline{S}_D$)
- Open-drain output ($\overline{Q}_1$ to $\overline{Q}_{32}$)
- Serial data output for cascading (SQ_{32})
- Wide operating temperature range (Ta = –40 to +85°C)
- Pin configuration for easy layout on PCB.
  (Pin configuration allows easy cascade connection or LED connection)

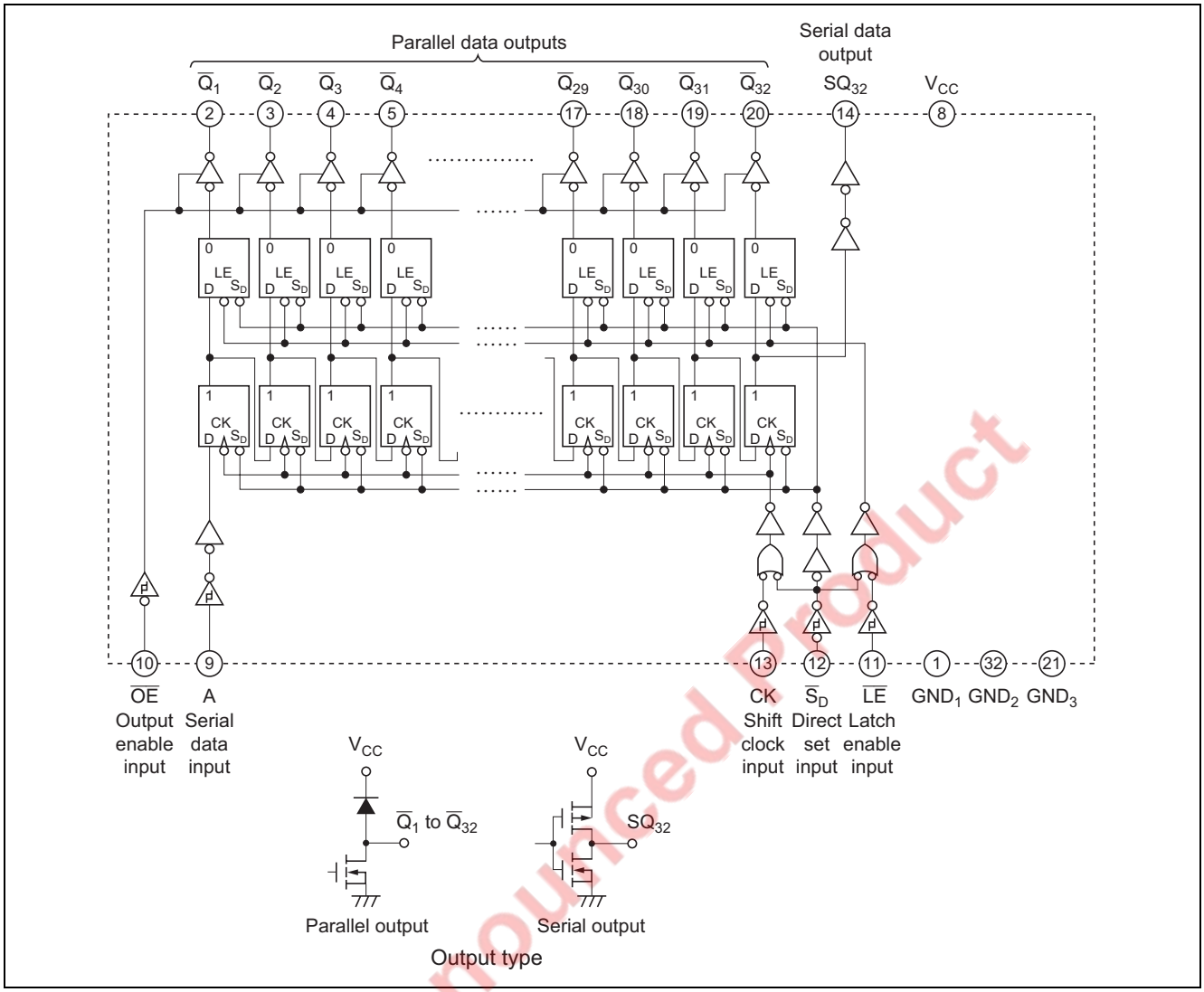
Application

LED array drive for eraser unit of a copying machine

LED array drive of a button telephone set

Various LED modules

Block Diagram



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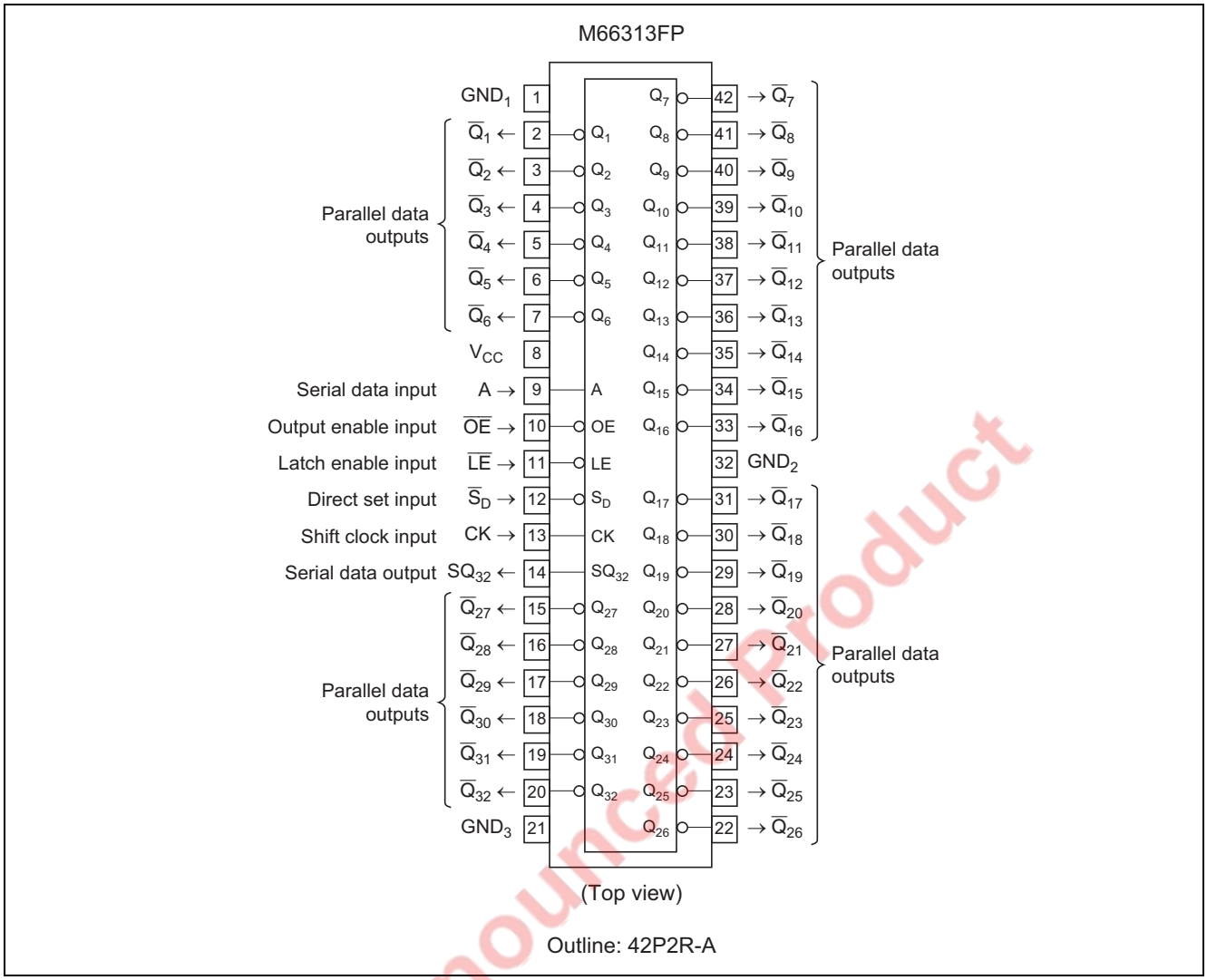
Pin Arrangement



Outline: 42P2R-A

Functional Description

The employment of silicon gate CMOS process of the M66313FP guarantees low power dissipation and maintains high noise margin as well as high output current and high speed required to drive LEDs.

Each shift register bit consists of a flip-flop for shifting and an output latch.

The shift operation takes place when the clock input CK changes from low-level to high-level.

The serial data input A corresponds to the data input of the first-stage shift register, and the shift register is shifted in sequence when a pulse is applied to CK.

The parallel outputs $\overline{Q}_1$ to $\overline{Q}_{32}$ are open-drain outputs.

If the latch-enable input $\overline{LE}$ is turned high–level, the content of the shift register at that instant is latched.

To expand the number of bits, use the serial data output SQ_{32} which shows the output of the shift register of the 32nd bit.

If the direct set input $\overline{S}_D$ is turned low-level, shift register and latches are set.

If the high-level input is applied to the output enable input $\overline{OE}$, $\overline{Q}_1$ to $\overline{Q}_{32}$ are set to the high-impedance state, but SQ_{32} is not set to the high-impedance state. The shift operation is not affected when $\overline{OE}$ is changed.

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Function Table (Note)

Operation Mode	Input					Parallel Data Output																																				Serial Data Output
	$\overline{S_D}$	CK	$\overline{LE}$	A	$\overline{OE}$	$\overline{Q}_1$	$\overline{Q}_2$	$\overline{Q}_3$	$\overline{Q}_4$	$\overline{Q}_5$	$\overline{Q}_6$	$\overline{Q}_7$	$\overline{Q}_8$	$\overline{Q}_9$	$\overline{Q}_{10}$	$\overline{Q}_{11}$	$\overline{Q}_{12}$	$\overline{Q}_{13}$	$\overline{Q}_{14}$	$\overline{Q}_{15}$	$\overline{Q}_{16}$	$\overline{Q}_{17}$	$\overline{Q}_{18}$	$\overline{Q}_{19}$	$\overline{Q}_{20}$	$\overline{Q}_{21}$	$\overline{Q}_{22}$	$\overline{Q}_{23}$	$\overline{Q}_{24}$	$\overline{Q}_{25}$	$\overline{Q}_{26}$	$\overline{Q}_{27}$	$\overline{Q}_{28}$	$\overline{Q}_{29}$	$\overline{Q}_{30}$	$\overline{Q}_{31}$	$\overline{Q}_{32}$	SQ_{32}
Set	L	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H
Shift	H	↑	L	H	L	L	$\overline{Q}^0_1$	$\overline{Q}^0_2$	$\overline{Q}^0_3$	$\overline{Q}^0_4$	$\overline{Q}^0_5$	$\overline{Q}^0_6$	$\overline{Q}^0_7$	$\overline{Q}^0_8$	$\overline{Q}^0_9$	$\overline{Q}^0_{10}$	$\overline{Q}^0_{11}$	$\overline{Q}^0_{12}$	$\overline{Q}^0_{13}$	$\overline{Q}^0_{14}$	$\overline{Q}^0_{15}$	$\overline{Q}^0_{16}$	$\overline{Q}^0_{17}$	$\overline{Q}^0_{18}$	$\overline{Q}^0_{19}$	$\overline{Q}^0_{20}$	$\overline{Q}^0_{21}$	$\overline{Q}^0_{22}$	$\overline{Q}^0_{23}$	$\overline{Q}^0_{24}$	$\overline{Q}^0_{25}$	$\overline{Q}^0_{26}$	$\overline{Q}^0_{27}$	$\overline{Q}^0_{28}$	$\overline{Q}^0_{29}$	$\overline{Q}^0_{30}$	$\overline{Q}^0_{31}$	q^0_{31}
	H	↑	L	L	L	Z	$\overline{Q}^0_1$	$\overline{Q}^0_2$	$\overline{Q}^0_3$	$\overline{Q}^0_4$	$\overline{Q}^0_5$	$\overline{Q}^0_6$	$\overline{Q}^0_7$	$\overline{Q}^0_8$	$\overline{Q}^0_9$	$\overline{Q}^0_{10}$	$\overline{Q}^0_{11}$	$\overline{Q}^0_{12}$	$\overline{Q}^0_{13}$	$\overline{Q}^0_{14}$	$\overline{Q}^0_{15}$	$\overline{Q}^0_{16}$	$\overline{Q}^0_{17}$	$\overline{Q}^0_{18}$	$\overline{Q}^0_{19}$	$\overline{Q}^0_{20}$	$\overline{Q}^0_{21}$	$\overline{Q}^0_{22}$	$\overline{Q}^0_{23}$	$\overline{Q}^0_{24}$	$\overline{Q}^0_{25}$	$\overline{Q}^0_{26}$	$\overline{Q}^0_{27}$	$\overline{Q}^0_{28}$	$\overline{Q}^0_{29}$	$\overline{Q}^0_{30}$	$\overline{Q}^0_{31}$	q^0_{31}
Latch	H	X	H	X	L	$\overline{Q}^0_1$	$\overline{Q}^0_2$	$\overline{Q}^0_3$	$\overline{Q}^0_4$	$\overline{Q}^0_5$	$\overline{Q}^0_6$	$\overline{Q}^0_7$	$\overline{Q}^0_8$	$\overline{Q}^0_9$	$\overline{Q}^0_{10}$	$\overline{Q}^0_{11}$	$\overline{Q}^0_{12}$	$\overline{Q}^0_{13}$	$\overline{Q}^0_{14}$	$\overline{Q}^0_{15}$	$\overline{Q}^0_{16}$	$\overline{Q}^0_{17}$	$\overline{Q}^0_{18}$	$\overline{Q}^0_{19}$	$\overline{Q}^0_{20}$	$\overline{Q}^0_{21}$	$\overline{Q}^0_{22}$	$\overline{Q}^0_{23}$	$\overline{Q}^0_{24}$	$\overline{Q}^0_{25}$	$\overline{Q}^0_{26}$	$\overline{Q}^0_{27}$	$\overline{Q}^0_{28}$	$\overline{Q}^0_{29}$	$\overline{Q}^0_{30}$	$\overline{Q}^0_{31}$	$\overline{Q}^0_{32}$	q_{32}
Output disable	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	q_{32}

Note ↑: Transition from low-to-high-level.
$\overline{Q}^0$: Shows the status of output $\overline{Q}$ before CK input changes.
X: Irrelevant
q^0: The content of shift register before CK changes.
q: The content of the shift register.
Z: High-impedance state.

Absolute Maximum Ratings

(Ta = –40 to +85°C, unless otherwise noted)

Item		Symbol	Ratings	Unit	Conditions
Supply voltage		V_{CC}	–0.5 to + 7.0	V	
Input voltage		V_I	–0.5 to V_{CC} + 0.5	V	
Output voltage		V_O	–0.5 to V_{CC} + 0.5	V	
Input protection diode current		I_{IK}	–20	mA	V_I < 0 V
			20		V_I > V_{CC}
Output parasitic diode current		I_{OK}	–20	mA	V_O < 0 V
			20		V_O > V_{CC}
Output current	$\overline{Q}_1$ to $\overline{Q}_{32}$	I_O	50	mA	
	SQ_{32}		±25		
Supply/GND current		I_{CC}	–920, +20	mA	V_{CC}, GND
Power dissipation		Pd	650	mW	
Storage temperature range		Tstg	–65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Limits			Unit
		Min	Typ	Max	
Supply voltage	V_{CC}	4.5	5	5.5	V
Input voltage	V_I	0	—	V_{CC}	V
Output voltage	V_O	0	—	V_{CC}	V
Operating free–air ambient temperature range	Topr	–40	—	+85	°C

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Electrical Characteristics

(V_{CC} = 4.5 to 5.5 V, unless otherwise noted)

Item		Symbol	Limits					Unit	Conditions	
			Ta = 25°C			Ta = –40 to +85°C				
			Min	Typ (Note1)	Max	Min	Max			
Positive-going threshold voltage		V_{T+}	0.35×V_{CC}	2.8	0.7×V_{CC}	0.35×V_{CC}	0.7×V_{CC}	V	V_O = 0.1V, V_{CC}–0.1V $\|I_O\|$ = 20µA	
Negative-going threshold voltage		V_{T-}	0.2×V_{CC}	2	0.55×V_{CC}	0.2×V_{CC}	0.55×V_{CC}	V	V_O = 0.1V,V_{CC}–0.1V $\|I_O\|$ = 20µA	
High-level output voltage	SQ_{32}	V_{OH}	V_{CC}–0.1	—	—	V_{CC}–0.1	—	V	V_I = V_{T+},V_{T-} V_{CC} = 4.5V	I_{OH} = –20µA
			3.83	—	—	3.66	—			I_{OH} = –4mA
Low-level output voltage	$\overline{Q}_1$ to $\overline{Q}_{32}$	V_{OL}	—	—	0.1	—	0.1	V	V_I = V_{T+},V_{T-} V_{CC} = 4.5V	I_{OL} = 20µA
			—	0.20	0.41	—	0.50			I_{OL} = 24mA
			—	0.25	0.48	—	0.55 (Note 2)			I_{OL} = 28mA
	SQ_{32}		—	—	0.1	—	0.1			I_{OL} = 20µA
			—	—	0.44	—	0.53			I_{OL} = 4mA
High-level input current		I_{IH}	—	—	0.5	—	5.0	µA	V_I = V_{CC}, V_{CC} = 5.5V	
Low-level input current		I_{IL}	—	—	–0.5	—	–5.0	µA	V_I = GND, V_{CC} = 5.5V	
Maximum output leak current	$\overline{Q}_1$ to $\overline{Q}_{32}$	I_O	—	—	1.0	—	10.0	µA	V_I = V_{T+}, V_{T-} V_{CC} = 5.5V	V_O = V_{CC}
			—	—	–1.0	—	–10.0			V_O = GND
Quiescent state dissipation current		I_{CC}	—	—	40.0	—	400.0	µA	V_I = V_{CC}, GND, V_{CC} = 5.5V	

Note: 1. All typical values are at V_{CC} = 5 V, Ta = 25°C
2. Ta = –40 to +70°C

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Switching Characteristics

(V_{CC} = 5V)

Item		Symbol	Limits					Unit	Conditions
			Ta = 25°C			Ta = –40 to +85°C			
			Min	Typ	Max	Min	Max		
Maximum clock frequency		f_{max}	5	30	—	4	—	MHz	C_L = 50 pF
Output enable time to low-level	CK-$\overline{Q}_1$ to $\overline{Q}_{32}$ (Turned on)	t_{PZL}	—	35	150	—	200	ns	R_L = 1 kΩ (Note 2)
Output disable time from low-level	CK-$\overline{Q}_1$ to $\overline{Q}_{32}$ (Turned off)	t_{PLZ}	—	35	200	—	250	ns	
Low-to-high, high-to-low output propagation time	CK-SQ_{32}	t_{PLH}	—	35	100	—	130	ns	
		t_{PHL}	—	40	100	—	130	ns	
Output enable time to low-level	$\overline{S}_D$-Q_1 to $\overline{Q}_{32}$ (Turned on)	t_{PZL}	—	35	150	—	200	ns	
Low-to-high output propagation time	$\overline{S}_D$-SQ_{32}	t_{PLH}	—	40	100	—	130	ns	
Output enable time to low-level	$\overline{LE}$- $\overline{Q}_1$ to $\overline{Q}_{32}$ (Turned on)	t_{PZL}	—	30	100	—	130	ns	
Output disable time from low-level	$\overline{LE}$-$\overline{Q}_1$ to $\overline{Q}_{32}$ (Turned off)	t_{PLZ}	—	35	150	—	200	ns	
Output enable time to low-level	$\overline{OE}$-$\overline{Q}_1$ to $\overline{Q}_{32}$ (Turned on)	t_{PZL}	—	30	100	—	130	ns	
Output disable time from low-level	$\overline{OE}$-$\overline{Q}_1$ to $\overline{Q}_{32}$ (Turned off)	t_{PLZ}	—	35	150	—	200	ns	
Input capacitance		C_I	—	3	10	—	10	pF	
Output capacitance		C_O	—	6	15	—	15	pF	$\overline{OE}$–V_{CC}
Power dissipation capacitance (Note 1)		C_{PD}	—	160	—	—	—	pF	

Note 1. C_{PD} is the equivalent capacitance of IC calculated by the operating power dissipation without load. The operating power dissipation without load is given as follows.

$P_D = C_{PD} \bullet V_{CC}^2 \bullet f_I + I_{CC} \bullet V_{CC}$

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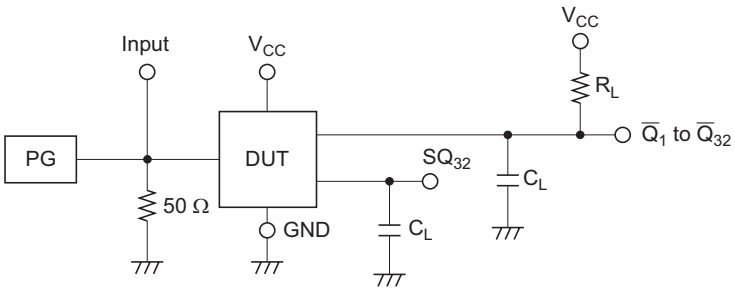
Timing Requirements

(V_{CC} = 5V)

Item	Symbol	Limits					Unit	Conditions
		Ta = 25°C			Ta = –40 to +85°C			
		Min	Typ	Max	Min	Max		
CK, $\overline{LE}$, $\overline{S}_D$ pulse width	t_W	100	16	—	130	—	ns	(Note 2)
Setup time A to CK	t_{su}	100	27	—	130	—	ns	
Hold time A to CK	t_h	10	5	—	15	—	ns	
Hold time $\overline{LE}$ to CK		50	15	—	70	—		
Recovery time CK to $\overline{S}_D$	t_{rec}	50	20	—	70	—	ns	

Note: 2. Test Circuit



(1) Characteristics of pulse generator (PG): tr = 6 ns, tf = 6 ns

(2) C_L includes probe and stray capacitance.

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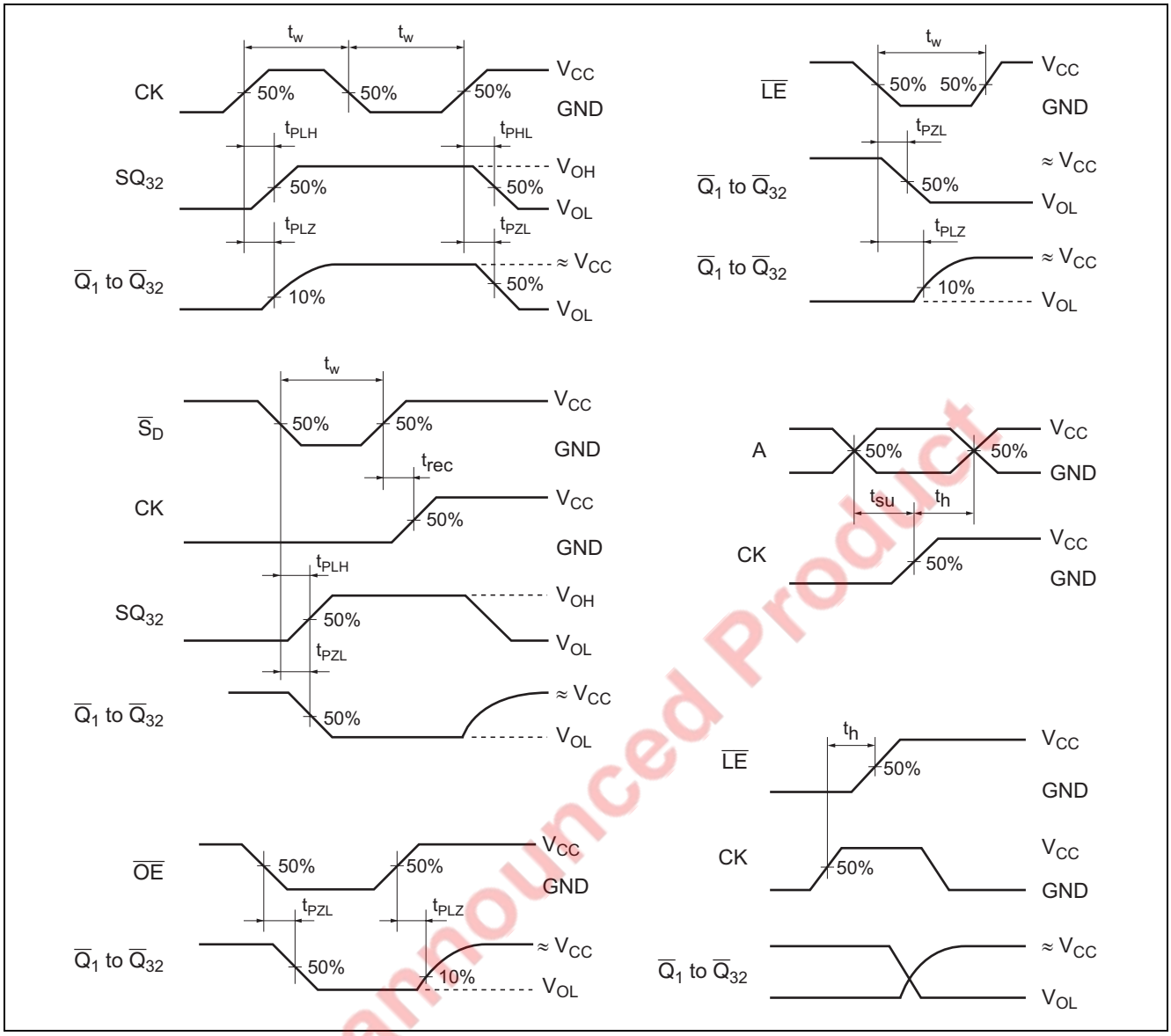
Timing Chart



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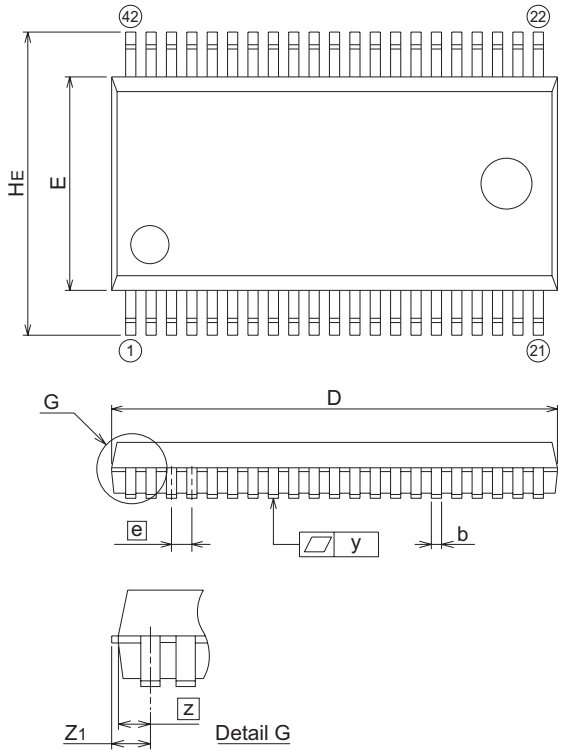
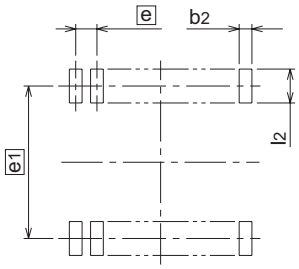
Package Dimensions

42P2R-A (MMP)

Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	—	0.63	Alloy 42/Cu Alloy





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A1	0.05	—	—
A2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	—	0.8	—
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	—	1.765	—
z	—	0.75	—
Z1	—	—	0.9
y	—	—	0.15
θ	0°	—	10°
b2	—	0.5	—
e1	—	11.43	—
l2	1.27	—	—

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