125°C OPERATION SPI SERIAL E^{2}PROM FOR AUTOMOTIVE ELECTRIC COMPONENT

S-25A640A

The S-25A640A is a SPI serial E^{2}PROM which operates under the high temperature, at high speed, with low current consumption and the wide range operation. The S-25A640A respectively has the capacity of 64 Kbit and the organization of 8192 words × 8-bit, is able to Page Write and sequential read.

■ Features

- Wide range operation Read: 2.5 V to 5.5 V
  Write: 2.5 V to 5.5 V
- Operation frequency 5.0 MHz (4.5 V to 5.5 V, at −40°C to +125°C)
- SPI mode (0, 0) and (1, 1)
- Page Write 32 bytes / page
- Sequential read
- Monitors Write to the memory by a status register
- Write protect: Software, Hardware
- Protect area: 25%, 50%, 100%
- Write protect function during the low power supply
- Function to prevent malfunction by monitoring clock pulse
- CMOS schmitt input ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)
- Endurance: 10^6cycles/word*1 (at +85°C)
  8×10^5 cycles/word*1 (at +105°C)
  5×10^5 cycles/word*1 (at +125°C)
  1. For each address (Word: 8-bit)
- Data retention: 100 years (at +25°C), 50 years (at +125°C)
- Memory capacitance: 64 Kbit
- Data before shipment: Memory array FFh, SRWD = 0, BP1 = 0, BP0 = 0
- Lead-free product

■ Package

Package name	Drawing code		
	Package	Tape	Reel
8-Pin SOP (JEDEC)	FJ008-A	FJ008-D	FJ008-D

Caution Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable.

■ Pin Configuration

8-Pin SOP (JEDEC)
Top view

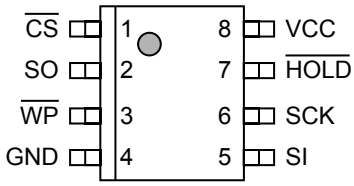


Figure 1

S-25A640A0A-J8T2UD
S-25A640A0H-J8T2UD

Table 1

Pin No.	Symbol	Description
1	$\overline{CS}$ *1	Chip select input
2	SO	Serial data output
3	$\overline{WP}$ *1	Write protect input
4	GND	Ground
5	SI*1	Serial data input
6	SCK*1	Serial clock input
7	$\overline{HOLD}$ *1	Hold input
8	VCC	Power supply

***1.** All input pins have the CMOS structure. Do not set the input pins in high impedance during operation.

Remark See Dimensions for details of the package drawings.

■ Block Diagram

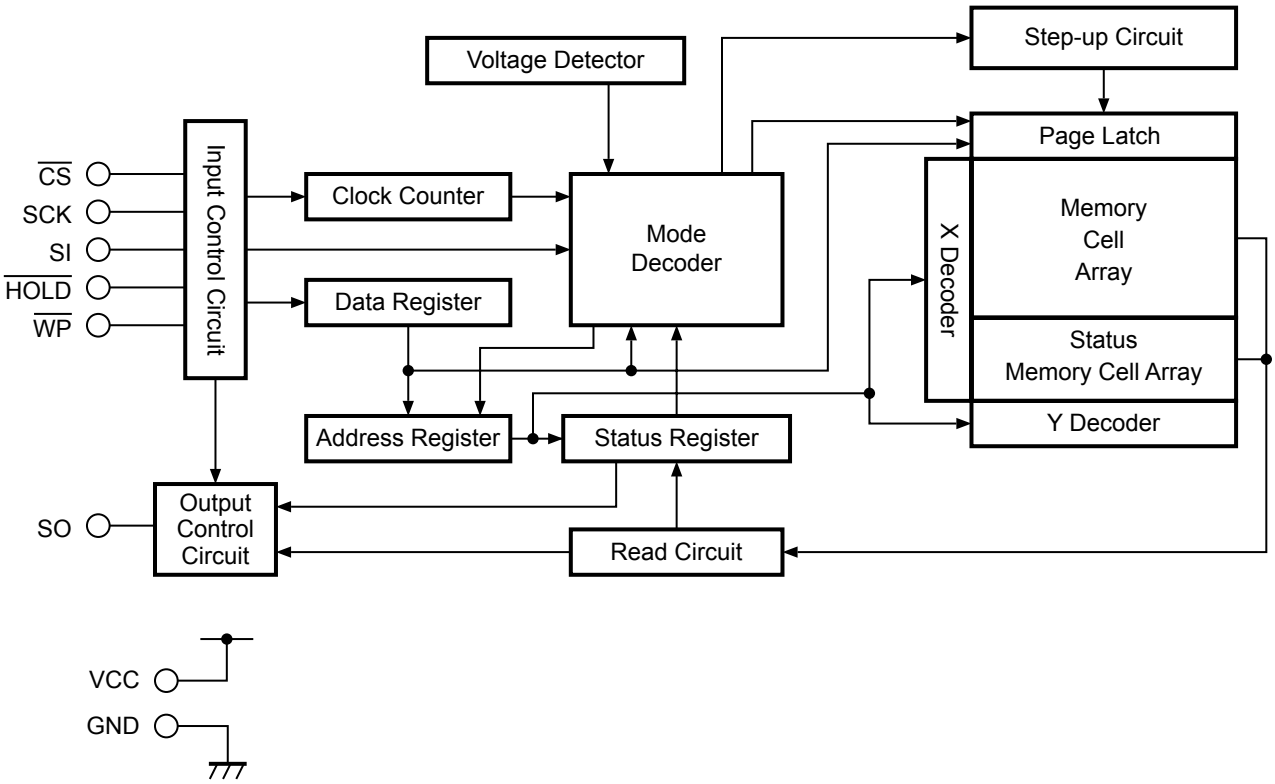


Figure 2

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to +7.0	V
Output voltage	V_{OUT}	−0.3 to V_{CC} + 0.3	V
Operation ambient temperature	T_{opr}	−40 to +125	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 3

Item	Symbol	Condition	Min.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation	2.5	5.5	V
		Write Operation	2.5	5.5	V
High level input voltage	V_{IH}	V_{CC} = 2.5 V to 5.5 V	0.7 × V_{CC}	V_{CC} + 1.0	V
Low level input voltage	V_{IL}	V_{CC} = 2.5 V to 5.5 V	−0.3	0.3 × V_{CC}	V

■ Pin Capacitance

Table 4

(Ta = +25 °C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	−	8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V (SO)	−	10	pF

■ Endurance

Table 5

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	−40°C to +85°C	10^6	−	cycles / word*1
		−40°C to +105°C	8.0×10^5	−	cycles / word*1
		−40°C to +125°C	5.0×10^5	−	cycles / word*1

***1.** For each address (Word: 8 bits)

■ Data Retention

Table 6

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	−	+25°C	100	−	year
		+125°C	50	−	year

■ DC Electrical Characteristics

Table 7

Item	Symbol	Condition	−40°C to +125°C						Unit
			V_{CC} = 2.5 V to 3.0 V f_{SCK} = 2.5 MHz		V_{CC} = 3.0 V to 4.5 V f_{SCK} = 3.5 MHz		V_{CC} = 4.5 V to 5.5 V f_{SCK} = 5.0 MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	No load at SO pin	−	1.5	−	2.0	−	2.5	mA

Table 8

Item	Symbol	Condition	−40°C to +125°C						Unit
			V_{CC} = 2.5 V to 3.0 V f_{SCK} = 2.5 MHz		V_{CC} = 3.0 V to 4.5 V f_{SCK} = 3.5 MHz		V_{CC} = 4.5 V to 5.5 V f_{SCK} = 5.0 MHz		
			Min.	Max.	Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I_{CC2}	No load at SO pin	−	4.0	−	5.0	−	6.0	mA

Table 9

Item	Symbol	Condition	−40°C to +85°C				+85°C to +125°C				Unit
			V_{CC} = 2.5 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		V_{CC} = 2.5 V to 4.5 V		V_{CC} = 4.5 V to 5.5 V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	$\overline{CS}$ = Vcc, SO = Open Other inputs are V_{CC} or GND	−	2.0	−	3.0	−	8.0	−	10.0	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−	1.0	−	1.0	−	2.0	−	2.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	−	1.0	−	1.0	−	2.0	−	2.0	μA
Low level output voltage	V_{OL1}	I_{OL} = 2.0 mA	−	−	−	0.4	−	−	−	0.4	V
	V_{OL2}	I_{OL} = 1.5 mA	−	0.4	−	0.4	−	0.4	−	0.4	V
High level output voltage	V_{OH1}	I_{OH} = −2.0 mA	−	−	0.8 × V_{CC}	−	−	−	0.8 × V_{CC}	−	V
	V_{OH2}	I_{OH} = −0.4 mA	0.8 × V_{CC}	−	0.8 × V_{CC}	−	0.8 × V_{CC}	−	0.8 × V_{CC}	−	V

■ AC Electrical Characteristics

Table 10 Measurement Conditions

Input pulse voltage	0.2 × V_{CC} to 0.8 × V_{CC}
Output reference voltage	0.5 × V_{CC}
Output load	100 pF

Table 11 S-25A640A0H (–40°C to +105°C)

Item	Symbol	–40°C to +105°C						Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 3.0 V to 5.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	f_{SCK}	–	3.5	–	5.0	–	5.0	MHz
$\overline{CS}$ setup time during $\overline{CS}$ falling	$t_{CSS.CL}$	90	–	90	–	90	–	ns
$\overline{CS}$ setup time during $\overline{CS}$ rising	$t_{CSS.CH}$	90	–	90	–	90	–	ns
$\overline{CS}$ deselect time	t_{CDS}	160	–	140	–	140	–	ns
$\overline{CS}$ hold time during $\overline{CS}$ falling	$t_{CSH.CL}$	90	–	90	–	90	–	ns
$\overline{CS}$ hold time during $\overline{CS}$ rising	$t_{CSH.CH}$	90	–	90	–	90	–	ns
SCK clock time "H" *1	t_{HIGH}	125	–	95	–	95	–	ns
SCK clock time "L" *1	t_{LOW}	125	–	95	–	95	–	ns
Rising time of SCK clock *2	t_{RSK}	–	1	–	1	–	1	µs
Falling time of SCK clock *2	t_{FSK}	–	1	–	1	–	1	µs
SI data input setup time	t_{DS}	20	–	20	–	20	–	ns
SI data input hold time	t_{DH}	30	–	30	–	30	–	ns
SCK "L" hold time during $\overline{HOLD}$ rising	$t_{SKH.HH}$	70	–	70	–	70	–	ns
SCL "L" hold time during $\overline{HOLD}$ falling	$t_{SKH.HL}$	40	–	40	–	40	–	ns
SCK "L" setup time during $\overline{HOLD}$ falling	$t_{SKS.HL}$	0	–	0	–	0	–	ns
SCK "L" setup time during $\overline{HOLD}$ rising	$t_{SKS.HH}$	0	–	0	–	0	–	ns
Disable time of SO output *2	t_{OZ}	–	100	–	100	–	100	ns
Delay time of SO output	t_{OD}	–	120	–	90	–	90	ns
Hold time of SO output	t_{OH}	0	–	0	–	0	–	ns
Rising time of SO output *2	t_{RO}	–	80	–	70	–	70	ns
Falling time of SO output *2	t_{FO}	–	80	–	70	–	70	ns
Disable time of SO output during $\overline{HOLD}$ falling *2	$t_{OZ.HL}$	–	100	–	100	–	100	ns
Delay time of SO output during $\overline{HOLD}$ rising *2	$t_{OD.HH}$	–	80	–	80	–	80	ns
$\overline{WP}$ setup time	t_{WS1}	0	–	0	–	0	–	ns
$\overline{WP}$ hold time	t_{WH1}	0	–	0	–	0	–	ns
$\overline{WP}$ release / setup time	t_{WS2}	0	–	0	–	0	–	ns
$\overline{WP}$ release / hold time	t_{WH2}	150	–	150	–	150	–	ns

***1.** The clock cycle of the SCK clock (frequency f_{SCK}) is $1/f_{SCK}$ µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as $(1/f_{SCK}) = t_{LOW}$ (Min.) + t_{HIGH} (Min.) by minimizing the SCK clock cycle time.

***2.** These are values of sample and not 100% tested.

Table 12 S-25A640A0A (–40°C to +125°C)

Item	Symbol	–40°C to +125°C						Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 3.0 V to 5.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	f_{SCK}	–	2.5	–	3.5	–	5.0	MHz
$\overline{CS}$ setup time during $\overline{CS}$ falling	$t_{CSS.CL}$	120	–	90	–	90	–	ns
$\overline{CS}$ setup time during $\overline{CS}$ rising	$t_{CSS.CH}$	120	–	90	–	90	–	ns
$\overline{CS}$ deselect time	t_{CDS}	210	–	160	–	140	–	ns
$\overline{CS}$ hold time during $\overline{CS}$ falling	$t_{CSH.CL}$	120	–	90	–	90	–	ns
$\overline{CS}$ hold time during $\overline{CS}$ rising	$t_{CSH.CH}$	120	–	90	–	90	–	ns
SCK clock time "H" *1	t_{HIGH}	160	–	125	–	95	–	ns
SCK clock time "L" *1	t_{LOW}	160	–	125	–	95	–	ns
Rising time of SCK clock *2	t_{RSK}	–	1	–	1	–	1	µs
Falling time of SCK clock *2	t_{FSK}	–	1	–	1	–	1	µs
SI data input setup time	t_{DS}	30	–	20	–	20	–	ns
SI data input hold time	t_{DH}	40	–	30	–	30	–	ns
SCK "L" hold time during $\overline{HOLD}$ rising	$t_{SKH.HH}$	90	–	70	–	70	–	ns
SCL "L" hold time during $\overline{HOLD}$ falling	$t_{SKH.HL}$	50	–	40	–	40	–	ns
SCK "L" setup time during $\overline{HOLD}$ falling	$t_{SKS.HL}$	0	–	0	–	0	–	ns
SCK "L" setup time during $\overline{HOLD}$ rising	$t_{SKS.HH}$	0	–	0	–	0	–	ns
Disable time of SO output *2	t_{OZ}	–	130	–	100	–	100	ns
Delay time of SO output	t_{OD}	–	160	–	120	–	90	ns
Hold time of SO output	t_{OH}	0	–	0	–	0	–	ns
Rising time of SO output *2	t_{RO}	–	110	–	80	–	80	ns
Falling time of SO output *2	t_{FO}	–	110	–	80	–	80	ns
Disable time of SO output during $\overline{HOLD}$ falling *2	$t_{OZ.HL}$	–	130	–	100	–	100	ns
Delay time of SO output during $\overline{HOLD}$ rising *2	$t_{OD.HH}$	–	110	–	80	–	80	ns
$\overline{WP}$ setup time	t_{WS1}	0	–	0	–	0	–	ns
$\overline{WP}$ hold time	t_{WH1}	0	–	0	–	0	–	ns
$\overline{WP}$ release / setup time	t_{WS2}	0	–	0	–	0	–	ns
$\overline{WP}$ release / hold time	t_{WH2}	200	–	150	–	150	–	ns

*1. The clock cycle of the SCK clock (frequency f_{SCK}) is $1/f_{SCK}$ µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as $(1/f_{SCK}) = t_{LOW}$ (Min.) + t_{HIGH} (Min.) by minimizing the SCK clock cycle time.

*2. These are values of sample and not 100% tested.

Table 13 S-25A640A0H, S-25A640A0A (–40°C to +85°C)

Item	Symbol	–40°C to +85°C						Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 3.0 V to 5.5 V		V_{CC} = 4.5 V to 5.5 V		
		Min.	Max.	Min.	Max.	Min.	Max.	
SCK clock frequency	f_{SCK}	–	3.5	–	5.0	–	5.0	MHz
$\overline{CS}$ setup time during $\overline{CS}$ falling	$t_{CSS.CL}$	90	–	90	–	90	–	ns
$\overline{CS}$ setup time during $\overline{CS}$ rising	$t_{CSS.CH}$	90	–	90	–	90	–	ns
$\overline{CS}$ deselect time	t_{CDS}	160	–	140	–	140	–	ns
$\overline{CS}$ hold time during $\overline{CS}$ falling	$t_{CSH.CL}$	90	–	90	–	90	–	ns
$\overline{CS}$ hold time during $\overline{CS}$ rising	$t_{CSH.CH}$	90	–	90	–	90	–	ns
SCK clock time "H" *1	t_{HIGH}	125	–	95	–	95	–	ns
SCK clock time "L" *1	t_{LOW}	125	–	95	–	95	–	ns
Rising time of SCK clock *2	t_{RSK}	–	1	–	1	–	1	µs
Falling time of SCK clock *2	t_{FSK}	–	1	–	1	–	1	µs
SI data input setup time	t_{DS}	20	–	20	–	20	–	ns
SI data input hold time	t_{DH}	30	–	30	–	30	–	ns
SCK "L" hold time during $\overline{HOLD}$ rising	$t_{SKH.HH}$	70	–	70	–	70	–	ns
SCL "L" hold time during $\overline{HOLD}$ falling	$t_{SKH.HL}$	40	–	40	–	40	–	ns
SCK "L" setup time during $\overline{HOLD}$ falling	$t_{SKS.HL}$	0	–	0	–	0	–	ns
SCK "L" setup time during $\overline{HOLD}$ rising	$t_{SKS.HH}$	0	–	0	–	0	–	ns
Disable time of SO output *2	t_{OZ}	–	100	–	100	–	100	ns
Delay time of SO output	t_{OD}	–	120	–	90	–	90	ns
Hold time of SO output	t_{OH}	0	–	0	–	0	–	ns
Rising time of SO output *2	t_{RO}	–	80	–	70	–	70	ns
Falling time of SO output *2	t_{FO}	–	80	–	70	–	70	ns
Disable time of SO output during $\overline{HOLD}$ falling *2	$t_{OZ.HL}$	–	100	–	100	–	100	ns
Delay time of SO output during $\overline{HOLD}$ rising *2	$t_{OD.HH}$	–	80	–	80	–	80	ns
$\overline{WP}$ setup time	t_{WS1}	0	–	0	–	0	–	ns
$\overline{WP}$ hold time	t_{WH1}	0	–	0	–	0	–	ns
$\overline{WP}$ release / setup time	t_{WS2}	0	–	0	–	0	–	ns
$\overline{WP}$ release / hold time	t_{WH2}	150	–	150	–	150	–	ns

***1.** The clock cycle of the SCK clock (frequency f_{SCK}) is $1/f_{SCK}$ µs. This clock cycle is determined by a combination of several AC characteristics. Note that the clock cycle cannot be set as $(1/f_{SCK}) = t_{LOW}$ (Min.) + t_{HIGH} (Min.) by minimizing the SCK clock cycle time.

***2.** These are values of sample and not 100% tested.

Table 14

Item	Symbol	−40°C to +125°C		Unit
		V_{CC} = 2.5 V to 5.5 V		
		Min.	Max.	
Write time	t_{PR}	–	4.0	ms

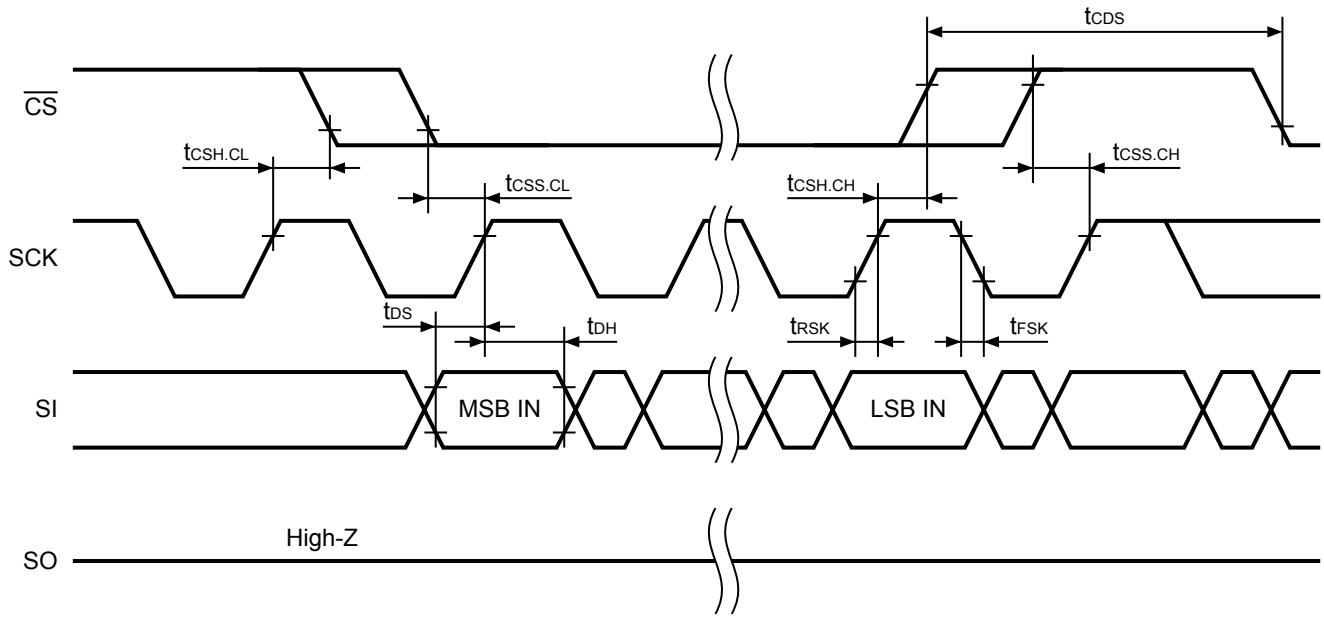


Figure 3 Serial Input Timing

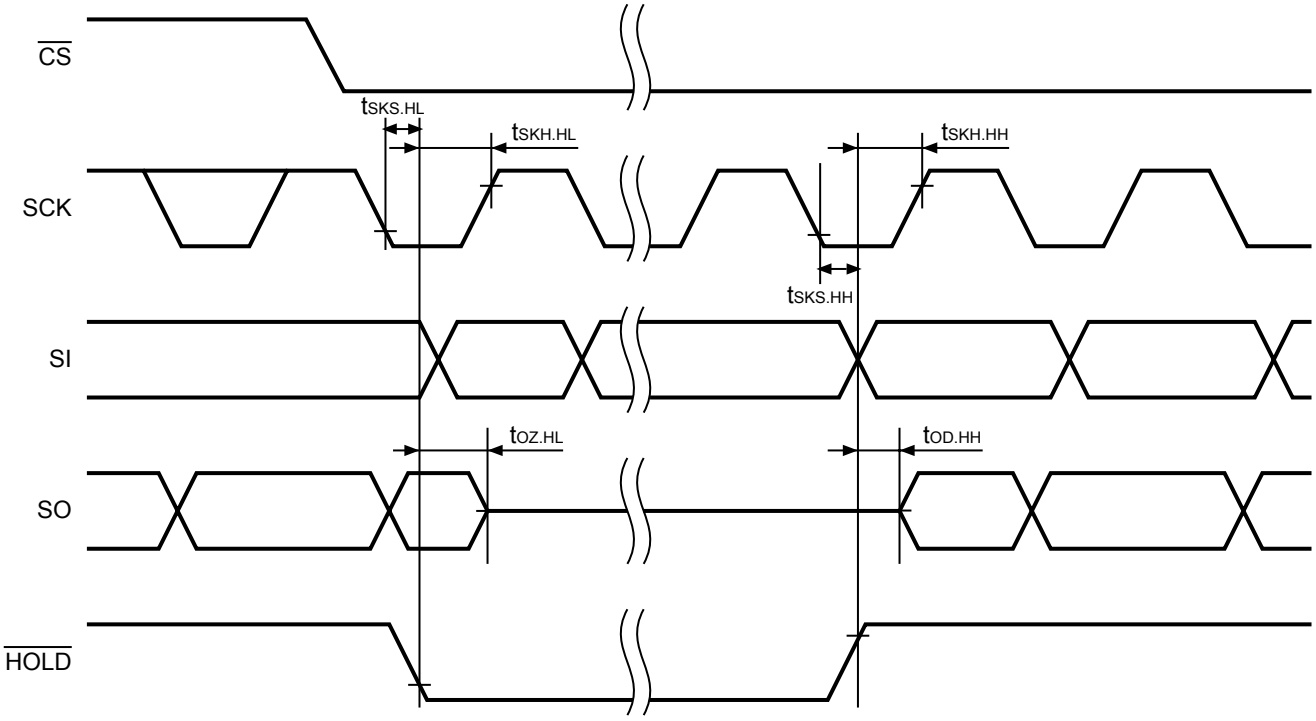


Figure 4 Hold Timing

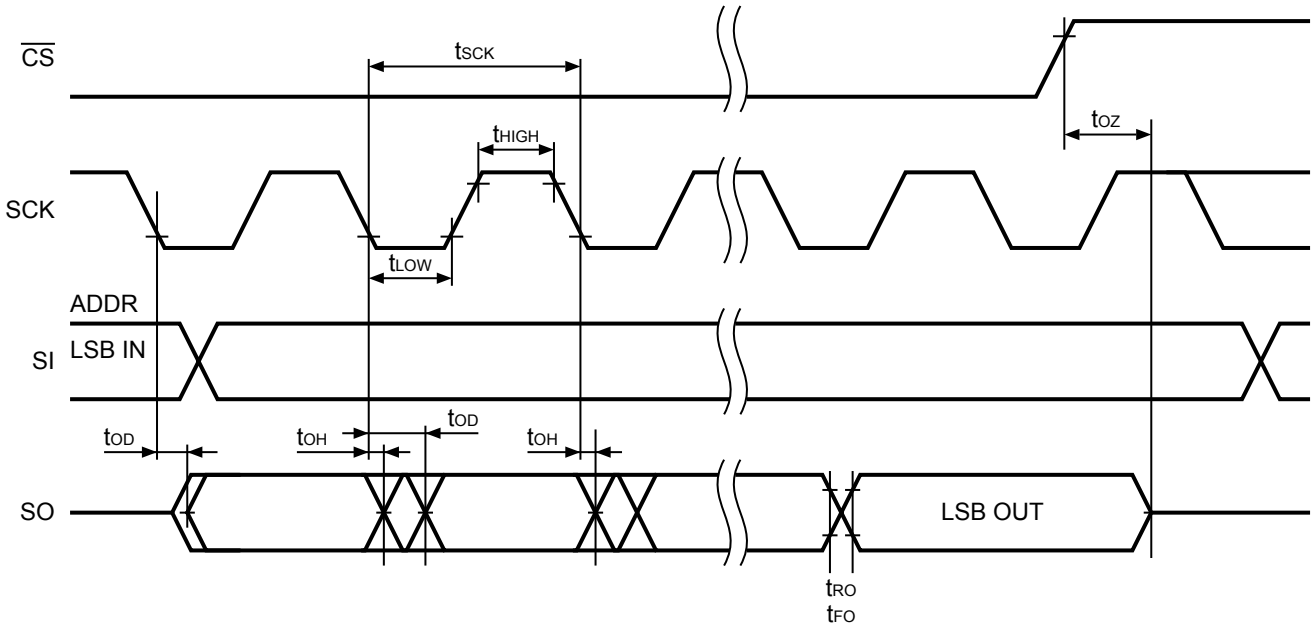


Figure 5 Serial Output Timing

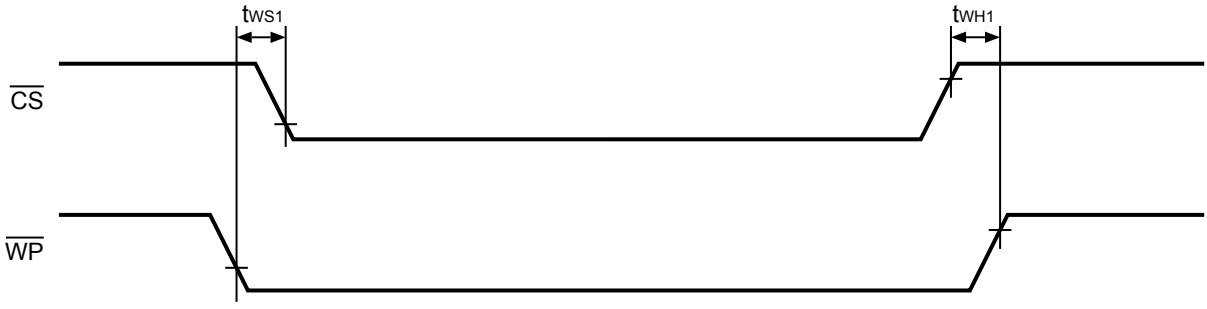


Figure 6 Valid Timing in Write Protect

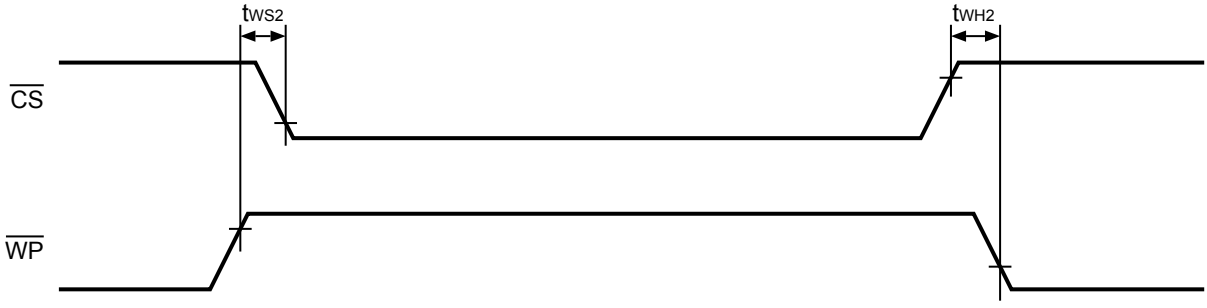


Figure 7 Invalid Timing in Write Protect

■ Pin Function

1. $\overline{CS}$ (Chip select input) Pin

This is an input pin to set a chip in the select status. In the “H” input level, the device is in the non-select status and its output is high impedance. The device is in standby as long as it is not in Write inside. The device goes in active by setting the chip select to “L”. Input any instruction code after power-on and a falling of chip select.

2. SI (Serial data input) pin

This pin is to input serial data. This pin receives an instruction code, an address and Write data. This pin latches data at rising edge of serial clock.

3. SO (Serial data output) pin

This pin is to output serial data. The data output changes at falling edge of serial clock.

4. SCK (Serial clock input) pin

This is a clock input pin to set the timing of serial data. An instruction code, an address and Write data are received at a rising edge of clock. Data is output at falling edge of clock.

5. $\overline{WP}$ (Write protect input) pin

Write protect is purposed to protect the area size against the Write instruction (BP1, BP0 in the status register). Fix this pin “H” or “L” not to set it in the floating state.
Refer to “■ **Protect Operation**” for details.

6. $\overline{HOLD}$ (HOLD input) pin

This pin is used to pause serial communications without setting the device in the non-select status.
In the hold status, the serial output goes in high impedance, the serial input and the serial clock go in “Don’t care”. During the hold operation, be sure to set the device in active by setting the chip select ($\overline{CS}$ pin) to “L”.
Refer to “■ **Hold Operation**” for details.

■ Instruction Setting

Table 15 is the list of instruction for the S-25A640A. The instruction is able to be input by changing the $\overline{CS}$ pin "H" to "L". Input the instruction in the MSB first. Each instruction code is organized with 1-byte as shown below. If the S-25A640A receives any invalid instruction code, the device goes in the non-select status.

Table 15

Instruction	Operation	Instruction code	Address		Data
		SCK input clock 1 to 8	SCK input clock 9 to 16	SCK input clock 17 to 24	SCK input clock 25 to 32
WREN	Write enable	0000 0110	–	–	–
WRDI	Write disable	0000 0100	–	–	–
RDSR	Read the status register	0000 0101	b7 to b0 output *1	–	–
WRSR	Write in the status register	0000 0001	b7 to b0 input	–	–
READ	Read memory data	0000 0011	A15 to A8 *2	A7 to A0	D7 to D0 output *3
WRITE	Write memory data	0000 0010	A15 to A8 *2	A7 to A0	D7 to D0 input

***1.** Sequential data reading is possible.
***2.** The higher addresses A15 to A13 = Don't care.
***3.** After outputting data in the specified address, data in the following address is output.

■ Operation

1. Status register

The status register's organization is below. The status register can Write and Read by a specific instruction.

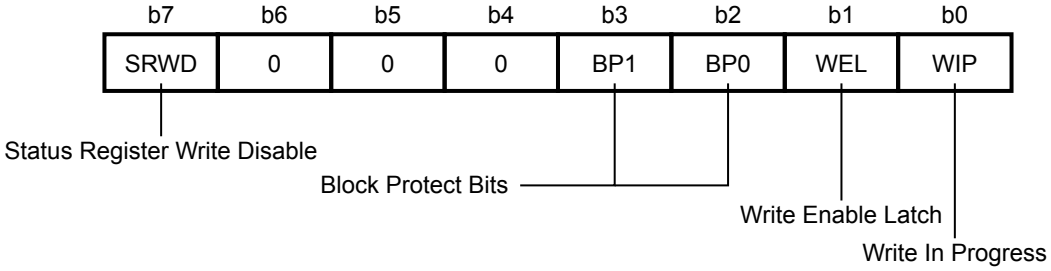


Figure 8 Organization of Status Register

The status/control bits of the status register are as follows.

1. 1 SRWD (b7) : Status Register Write Disable

Bit SRWD operates in conjunction with the Write protect signal ($\overline{WP}$). With a combination of bit SRWD and signal $\overline{WP}$ (SRWD = "1", $\overline{WP}$ = "L"), this device goes in Hardware Protect status. In this case, the bits composed of the nonvolatile bit in the status register (SRWD, BP1, BP0) go in Read Only, so that the WRSR instruction is not be performed.

1. 2 BP1, BP0 (b3, b2) : Block Protect

Bit BP1 and BP0 are composed of the nonvolatile bit. The area size of Software Protect against WRITE instruction is defined by them. Rewriting these bits is possible by the WRSR instruction. To protect the memory area against the WRITE instruction, set either or both of bit BP1 and BP0 to "1". Rewriting bit BP1 and BP0 is possible unless they are in Hardware Protect mode. Refer to "■ **Protect Operation**" for details of "Block Protect".

1. 3 WEL (b1) : Write Enable Latch

Bit WEL shows the status of internal Write Enable Latch. Bit WEL is set by the WREN instruction only. If bit WEL is "1", this is the status that Write Enable Latch is set. If bit WEL is "0", Write Enable Latch is in reset, so that the S-25A640A does not receive the WRITE or WRSR instruction. Bit WEL is reset after these operations;

- The power supply voltage is dropping
- Power-on
- After performing WRDI
- After the Write operation by the WRSR instruction
- After the Write operation by the WRITE instruction

1. 4 WIP (b0) : Write In Progress

Bit WIP is Read Only and shows whether the internal memory is in the Write operation or not by the WRITE or WRSR instruction. Bit WIP is "1" during the Write operation but "0" during any other status. **Figure 9** shows the usage example.

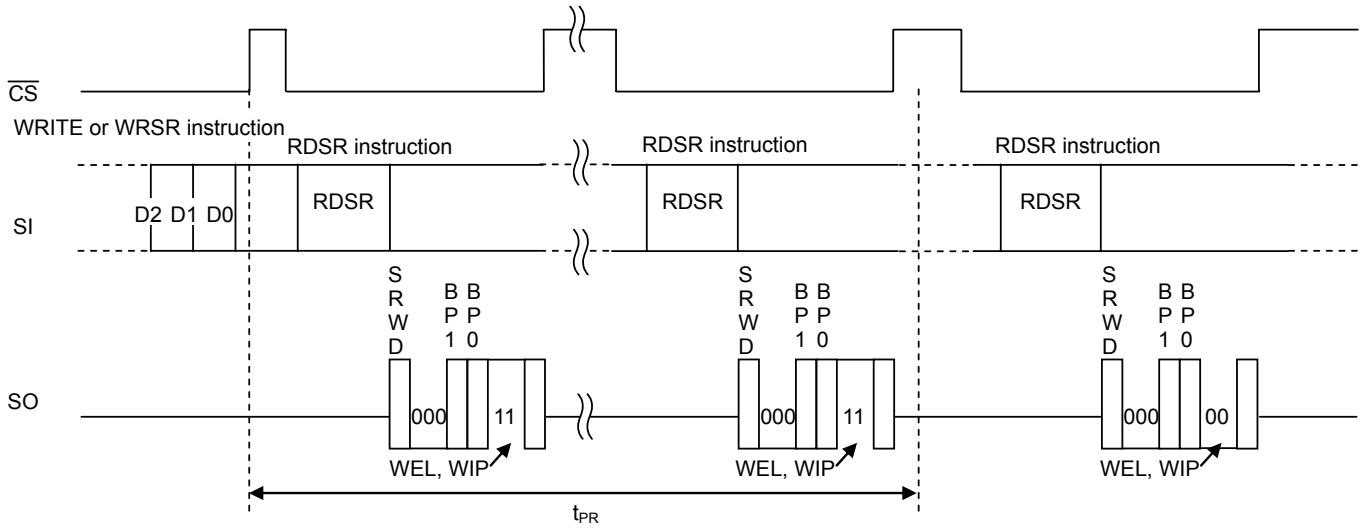


Figure 9 Usage Example of WEL, WIP Bits during Write

2. Write enable (WREN)

Before writing data (WRITE and WRSR), be sure to set bit Write Enable Latch (WEL). This instruction is to set bit WEL. Its operation is below.

After selecting the device by the chip select ($\overline{CS}$), input the instruction code from serial data input (SI). To set bit WEL, set the device in the non-select status by $\overline{CS}$ at the 8th clock of the serial clock (SCK). To cancel the WREN instruction, input the clock different from a specified value (n = 8 clock) while $\overline{CS}$ is in "L".

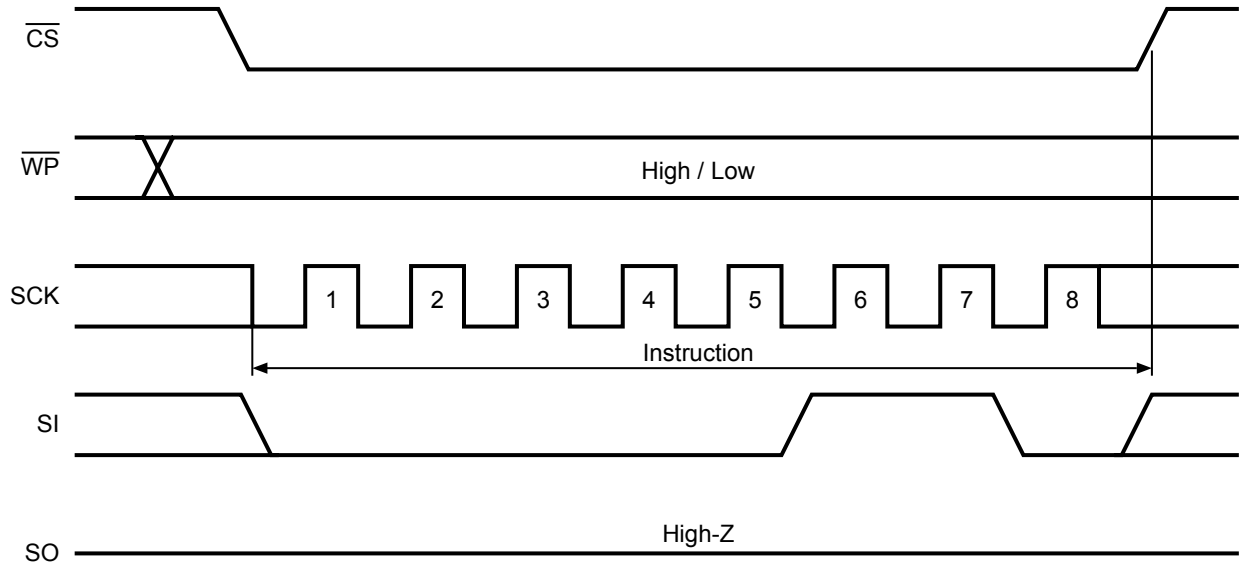


Figure 10 WREN Operation

3. Write disable (WRDI)

The WRDI instruction is one of ways to reset bit Write Enable Latch (WEL). After selecting the device by the chip select ($\overline{CS}$), input the instruction code from serial data input (SI).

To reset bit WEL, set the device in the non-select status by $\overline{CS}$ at the 8th clock of the serial clock. To cancel the WRDI instruction, input the clock different from a specified value (n = 8 clock) while $\overline{CS}$ is in "L". Bit WEL is reset after the operations shown below.

- The power supply voltage is dropping
- Power-on
- After performing WRDI
- After the completion of Write operation by the WRSR instruction
- After the completion of Write operation by the WRITE instruction

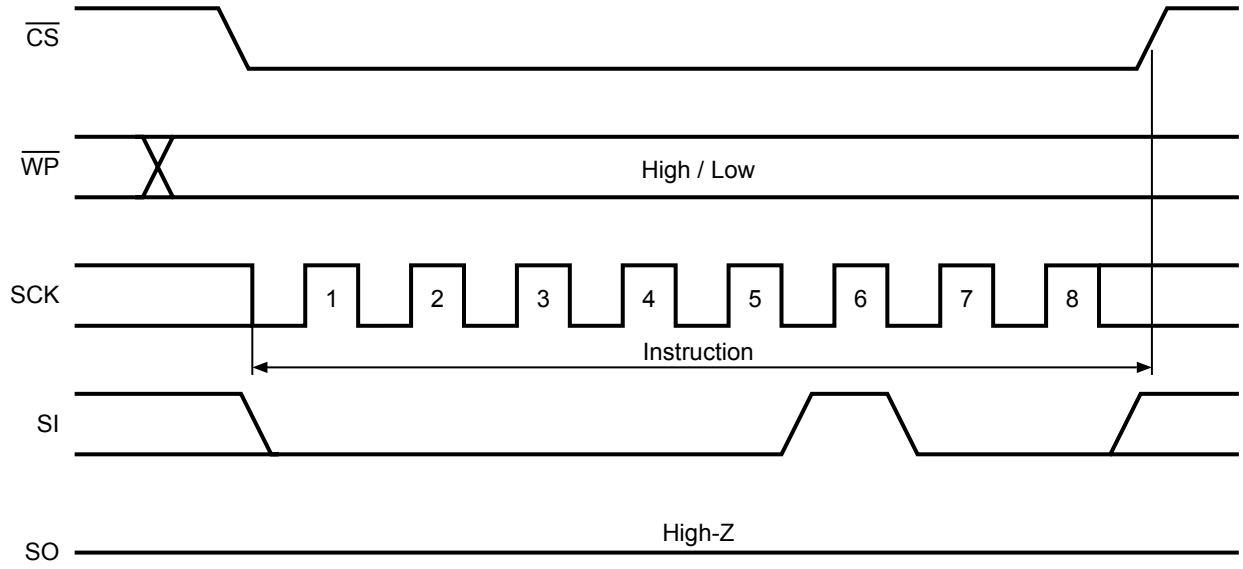


Figure 11 WRDI Operation

4. Read the status register (RDSR)

Reading data in the status register is possible by the RDSR instruction. During the Write operation, it is possible to confirm the progress by checking bit WIP.

Set the chip select ($\overline{CS}$) "L" first. After that, input the instruction code from serial data input (SI). The status of bit in the status register is output from serial data output (SO). Sequential Read is available for the status register. To stop the Read cycle, set $\overline{CS}$ to "H".

It is possible to read the status register always. The bits in it are valid and can be read by RDSR even in the Write cycle. However, during the Write cycle in progress, the nonvolatile bits SRWD, BP1, BP0 are fixed in a certain value. These updated values of bit can be obtained by inputting another new RDSR instruction after the Write cycle has completed. Contrarily, two of Read Only bits WEL and WIP are being updated while the Write cycle is in progress.

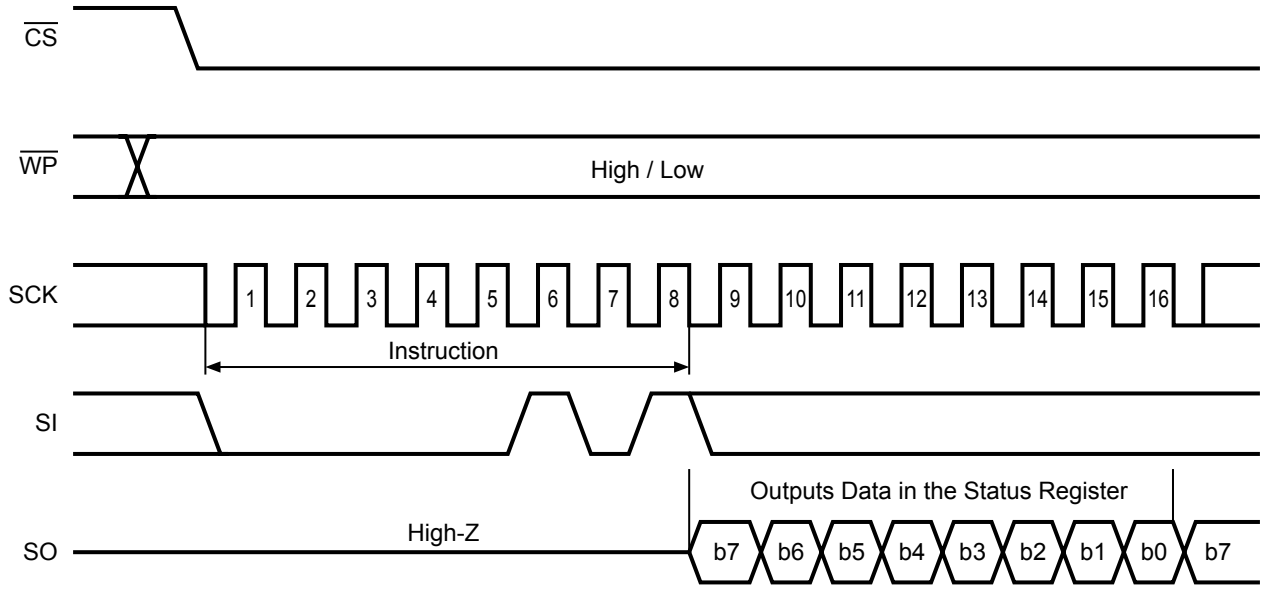


Figure 12 RDSR Operation

5. Write in the status register (WRSR)

The values of status register (SRWD, BP1, BP0) can be rewritten by inputting the WRSR instruction. But b6, b5, b4, b1, b0 of status register cannot be rewritten. b6 to b4 are always "0" when reading the status register.

Before inputting the WRSR instruction, set bit WEL by the WREN instruction. The operation of WRSR is shown below.

Set the chip select ($\overline{CS}$) "L" first. After that, input the instruction code and data from serial data input (SI). To start WRSR Write (t_{PR}), set the chip select ($\overline{CS}$) to "H" after inputting data or before inputting a rising of the next serial clock.

It is possible to confirm the operation status by reading the value of bit WIP during WRSR Write. Bit WIP is "1" during Write, "0" during any other status. Bit WEL is reset when Write is completed.

With the WRSR instruction, the values of BP1 and BP0; which determine the area size the users can handle as the Read Only memory; can be changed. Besides bit SRWD can be set or reset by the WRSR instruction depending on the status of Write protect $\overline{WP}$. With a combination of bit SRWD and Write protect $\overline{WP}$, the device can be set in Hardware Protect mode (HPM). In this case, the WRSR instruction is not be performed (Refer to "■ **Protect Operation**").

Bit SRWD and BP1, BP0 keep the value which is the one prior to the WRSR instruction during the WRSR instruction. The newly updated value is changed when the WRSR instruction has completed.

To cancel the WRSR instruction, input the clock different from a specified value (n = 16 clock) while $\overline{CS}$ is in "L".

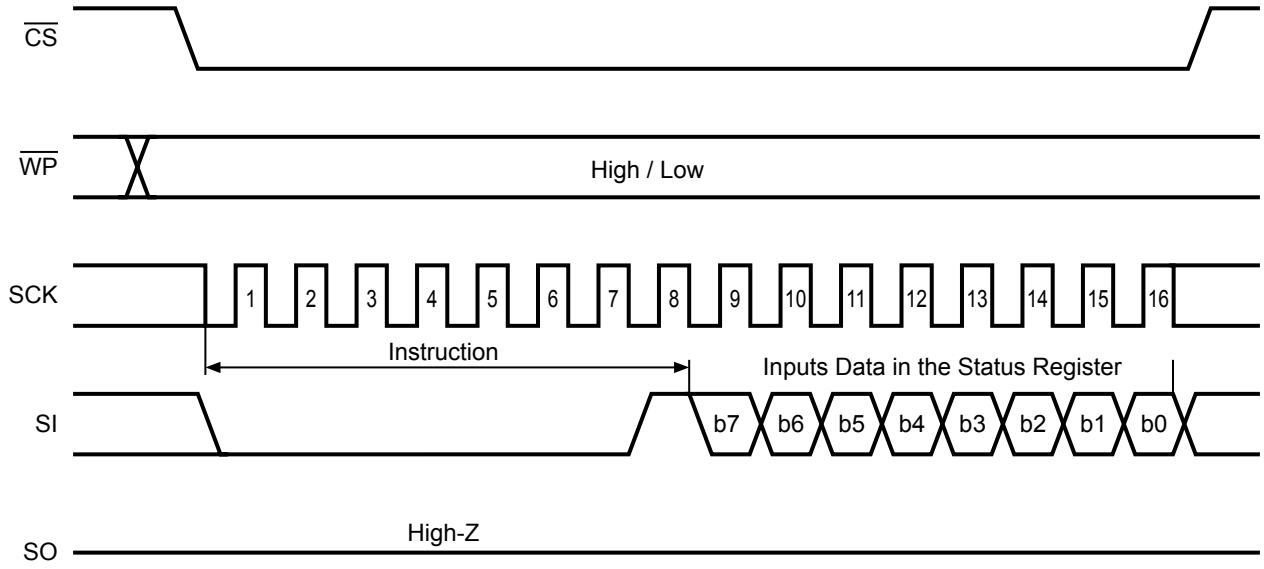


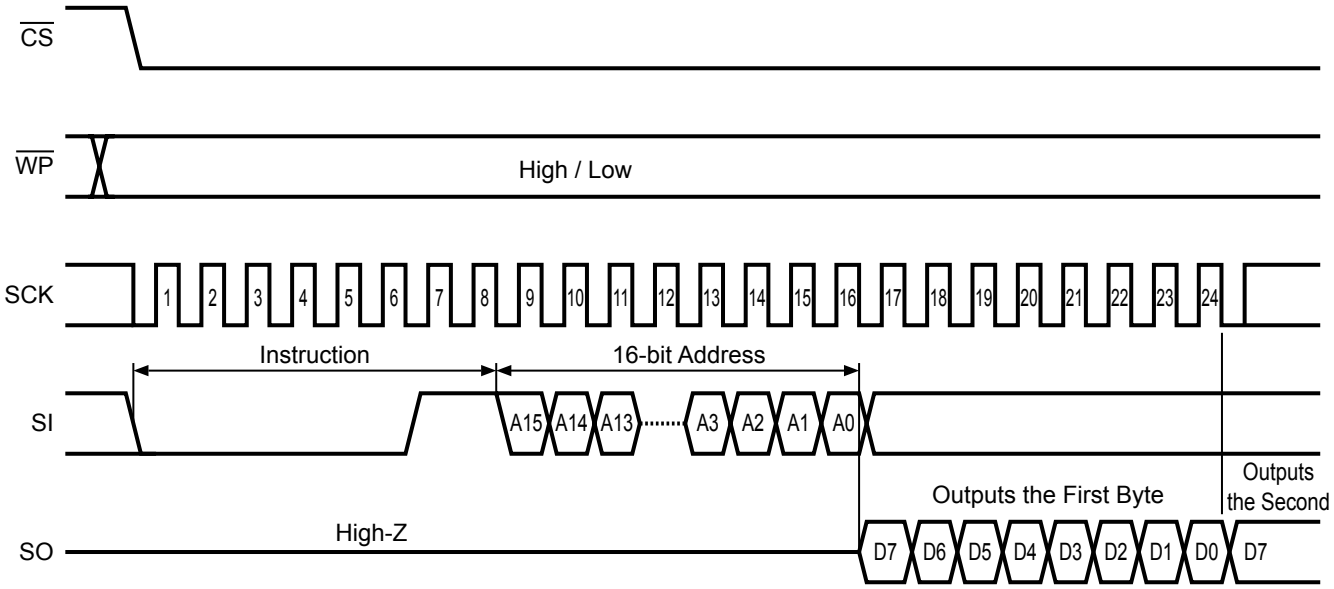
Figure 13 WRSR Operation

6. Read memory data (READ)

The Read operation is shown below. Input the instruction code and the address from serial data input (SI) after inputting "L" to the chip select ($\overline{CS}$). The input address is loaded to the internal address counter, and data in the address is output from the serial data output (SO).

Next, by inputting the serial clock (SCK) keeping the chip select ($\overline{CS}$) in "L", the address is automatically incremented so that data in the following address is sequentially output. The address counter rolls over to the first address by increment in the last address.

To finish the Read cycle, set $\overline{CS}$ to "H". It is possible to raise the chip select always during the cycle. During Write, the Read instruction code is not be accepted or operated.



Remark The higher addresses A15 to A13 = Don't care.

Figure 14 Read Operation

7. Write memory data (Write)

Figure 15 shows the timing chart when inputting 1-byte data. Input the instruction code, the address and data from serial data input (SI) after inputting "L" to the chip select ($\overline{CS}$). To start Write (t_{PR}), set the chip select ($\overline{CS}$) to "H" after inputting data or before inputting a rising of the next serial clock. Bit WIP and WEL are reset to "0" when Write has completed.

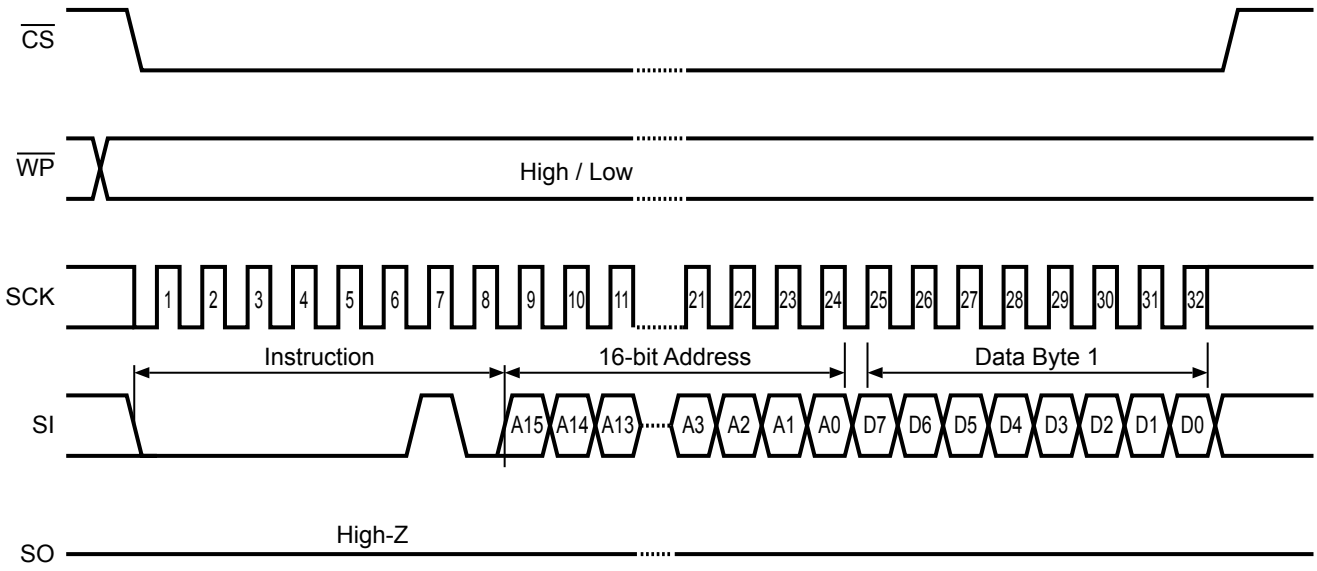
The S-25A640A can Page Write of 32 bytes. Its function to transmit data is as same as Byte Write basically, but it operates Page Write by receiving sequential 8-bit Write data as much data as page size has. Input the instruction code, the address and data from serial data input (SI) after inputting "L" in $\overline{CS}$, as the Write operation (page) shown in **Figure 16**. Input the next data while keeping $\overline{CS}$ in "L". After that, repeat inputting data of 8-bit sequentially. At the end, by setting $\overline{CS}$ to "H", the Write operation starts (t_{PR}).

5 of the lower bits in the address are automatically incremented every time when receiving Write data of 8-bit. Thus, even if Write data exceeds 32 bytes, the higher bits in the address do not change. And 5 of lower bits in the address roll over so that Write data which is previously input is overwritten.

These are cases when the Write instruction is not accepted or operated.

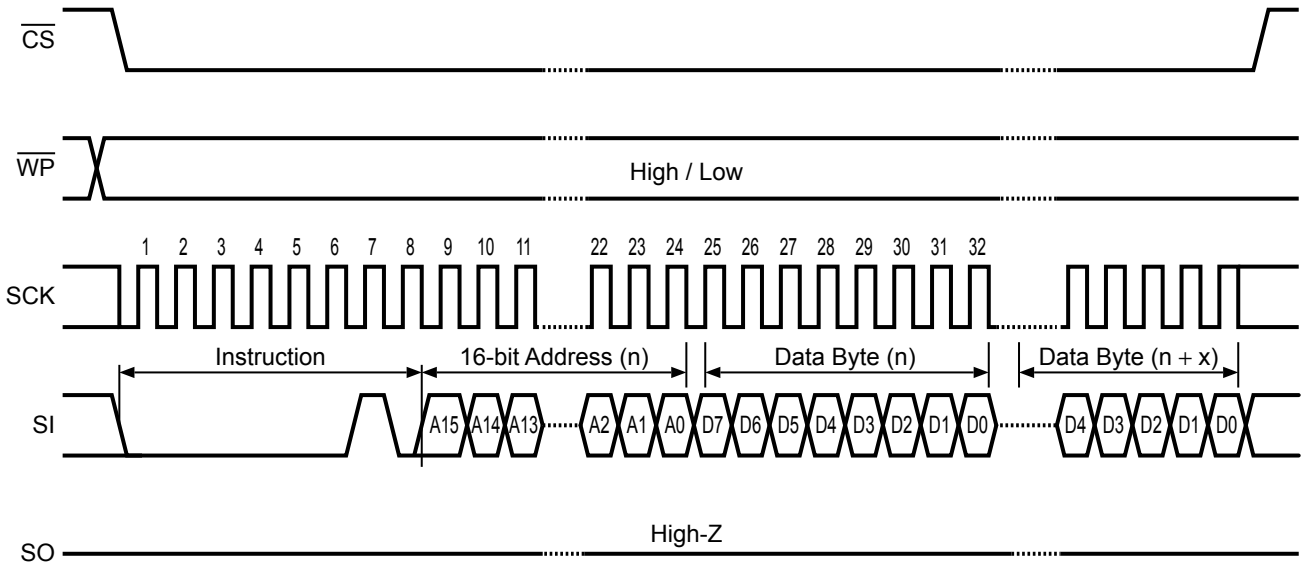
- Bit WEL is not set to "1" (not set to "1" beforehand immediately before the Write instruction)
- During Write
- The address to be written is in the protect area by BP1 and BP0.

To cancel the Write instruction, input the clock different from a specified value (n = 24+m × 8 clock) while $\overline{CS}$ is in "L".



Remark The higher addresses A15 to A13 = Don't care.

Figure 15 Write Operation (1 byte)



Remark The higher addresses A15 to A13 = Don't care.

Figure 16 Write Operation (Page)

■ Protect Operation

Table 16 shows the block settings of Write protect. **Table 17** shows the protect operation for the device. As long as bit SRWD, the Status Register Write Disable bit, in the status register is reset to "0" (it is in reset before the shipment), the value of status register can be changed.

These are two statuses when bit SRWD is set to "1".

- Write in the status register is possible; Write protect ($\overline{WP}$) is in "H".
- Write in the status register is impossible; Write protect ($\overline{WP}$) is in "L". Therefore the Write protect area which is set by protect bit (BP1, BP0) in the status register cannot be changed.

These operations are to set Hardware Protect (HPM).

- After setting bit SRWD, set Write protect ($\overline{WP}$) to "L".
- Set bit SRWD completed setting Write protect ($\overline{WP}$) to "L".

Figure 6 and **7** show the Valid timing in Write protect and Invalid timing in Write protect during the cycle Write to the status register.

By inputting "H" to Write protect ($\overline{WP}$), Hardware Protect (HPM) is released. If the Write protect ($\overline{WP}$) is "H", Hardware Protect (HPM) does not function, Software Protect (SPM) which is set by the protect bits in the status register (BP1, BP0) only works.

Table 16 The Block Settings of Write Protect

Status register		The area of Write protect	Address of Write protect block
BP1	BP0		
0	0	0 %	None
0	1	25 %	1800h to 1FFFh
1	0	50 %	1000h to 1FFFh
1	1	100 %	0000h to 1FFFh

Table 17 Protect Operation

Mode	$\overline{WP}$ pin	Bit SRWD	Bit WEL	Write protect block	General block	Status register
Software Protect (SPM)	1	X	0	Write disable	Write disable	Write disable
	1	X	1	Write disable	Write enable	Write enable
	X	0	0	Write disable	Write disable	Write disable
	X	0	1	Write disable	Write enable	Write enable
Hardware Protect (HPM)	0	1	0	Write disable	Write disable	Write disable
	0	1	1	Write disable	Write enable	Write disable

Remark X = Don't care

■ Hold Operation

The hold operation is used to pause serial communications without setting the device in the non-select status. In the hold status, the serial data output goes in high impedance, and both of the serial data input and the serial clock go in "Don't care". Be sure to set the chip select ($\overline{CS}$) to "L" to set the device in the select status during the hold status.
Generally, during the hold status, the device holds the select status. But if setting the device in the non-select status, the users can finish the operation even in progress.
Figure 17 shows the hold operation. Set Hold ($\overline{HOLD}$) to "L" when the serial clock (SCK) is in "L", Hold ($\overline{HOLD}$) is switched at the same time the hold status starts. If setting Hold ($\overline{HOLD}$) to "H", Hold ($\overline{HOLD}$) is switched at the same time the hold status ends.
Set Hold ($\overline{HOLD}$) to "L" when the serial clock (SCK) is in "H"; the hold status starts when the serial clock goes in "L" after Hold ($\overline{HOLD}$) is switched. If setting Hold ($\overline{HOLD}$) to "H", the hold status ends when the serial clock goes in "L" after Hold ($\overline{HOLD}$) is switched.

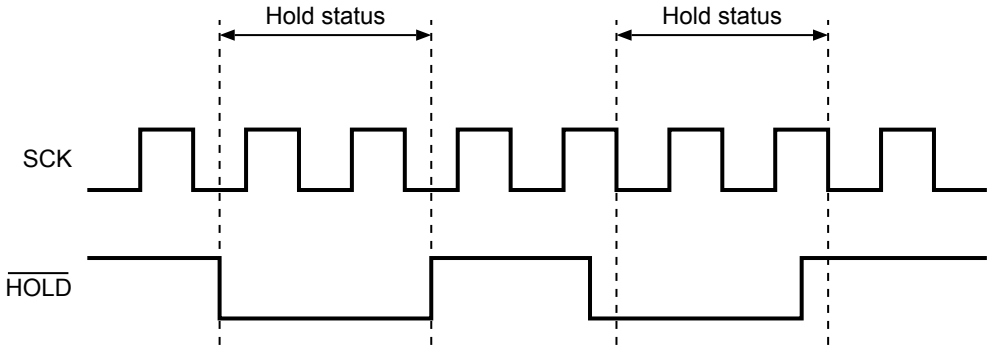


Figure 17 Hold Operation

■ Write Protect Function during the Low Power Supply Voltage

The S-25A640A has a built-in detection circuit which operates with the low power supply voltage. The S-25A640A cancels the Write operation (WRITE, WRSR) when the power supply voltage drops and power-on, at the same time, goes in the Write protect status (WRDI) automatically to reset bit WEL. The detection voltage is 1.20 V typ., the release voltage is 1.35 V typ., and its hysteresis is approx. 0.15 V (Refer to **Figure 18**).
To operate Write, after the power supply voltage dropped once but rose to the voltage level which allows Write again, be sure to set the Write Enable Latch bit (WEL) before operating Write (WRITE, WRSR).
In the Write operation, data in the address written during the low power supply voltage is not assured.

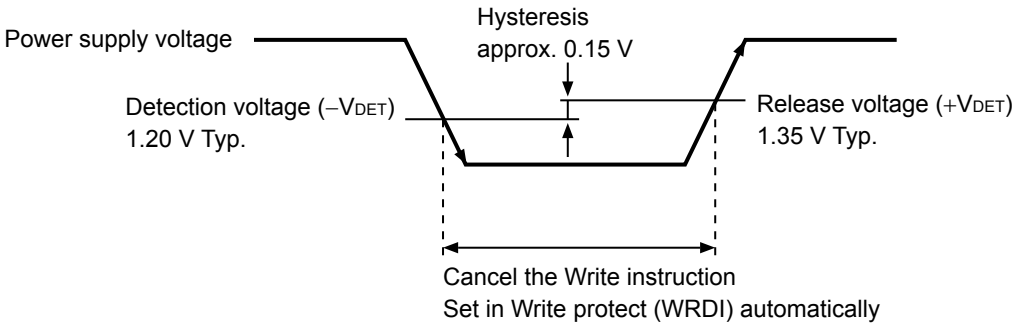


Figure 18 Operation during Low Power Supply Voltage

■ I/O Pin

1. Connection of input pin

All input pins in S-25A640A have the CMOS structure. Do not set these pins in high impedance during operation when you design. Especially, set the $\overline{CS}$ input in the non-select status "H" during power-on/off and standby. The error Write does not occur as long as the $\overline{CS}$ pin is in the non-select status "H". Set the $\overline{CS}$ pin to V_{CC} via a resistor (the pull-up resistor of 10 kΩ to 100 kΩ). To prevent the error for sure, it is recommended to set other input pins than the $\overline{CS}$ pin via a pull-up resistor.

2. Equivalent circuit of I/O pin

Figure 19 and **20** show the equivalent circuits of input pins in S-25A640A. A pull-up and pull-down elements are not included in each input pin, pay attention not to set it in the floating state when you design.
Figure 21 shows the equivalent circuit of the output pin. This pin has the tri-state output of "H" level/"L" level/high impedance.

2. 1 Input pin

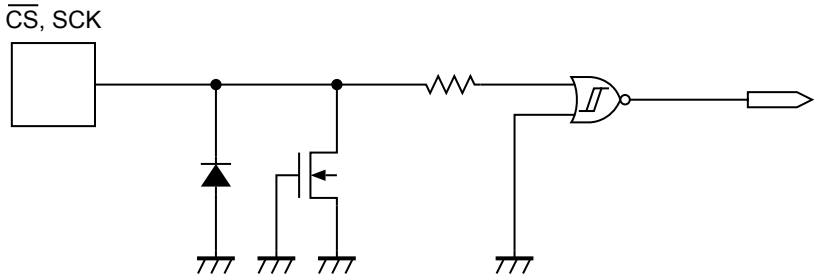


Figure 19 $\overline{CS}$, SCK Pin

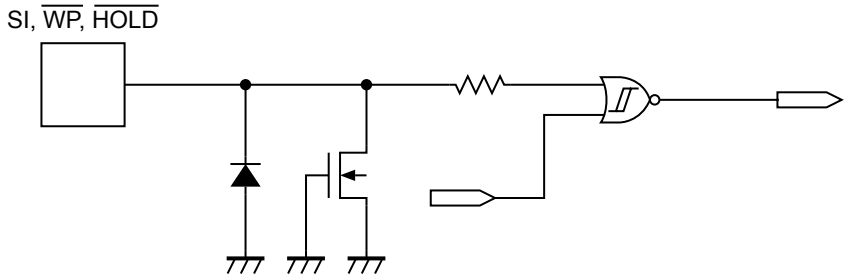


Figure 20 SI, $\overline{WP}$, $\overline{HOLD}$ Pin

2. 2 Output pin

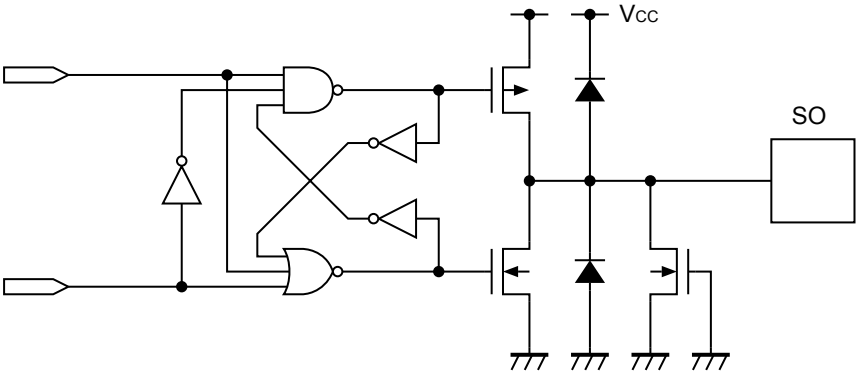


Figure 21 SO Pin

3. Precaution for use

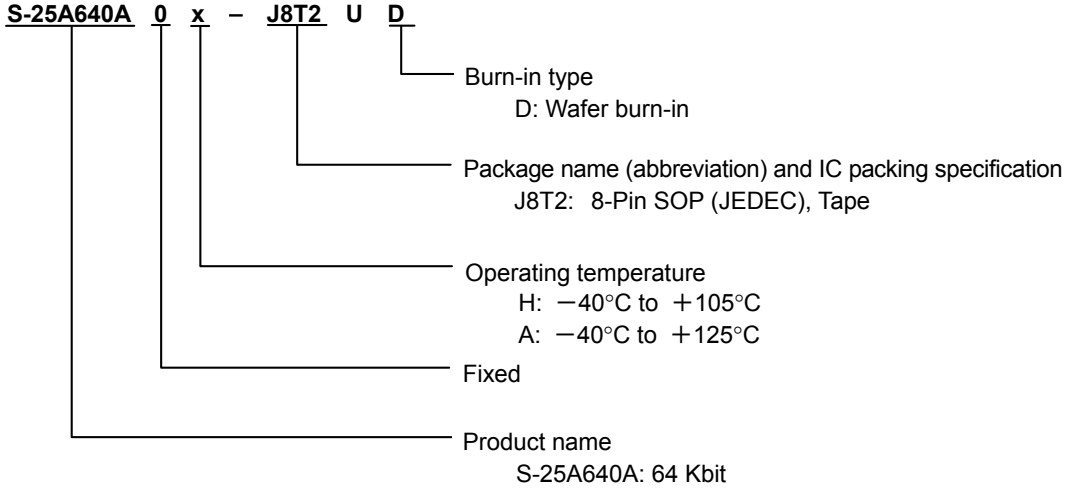
Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up.

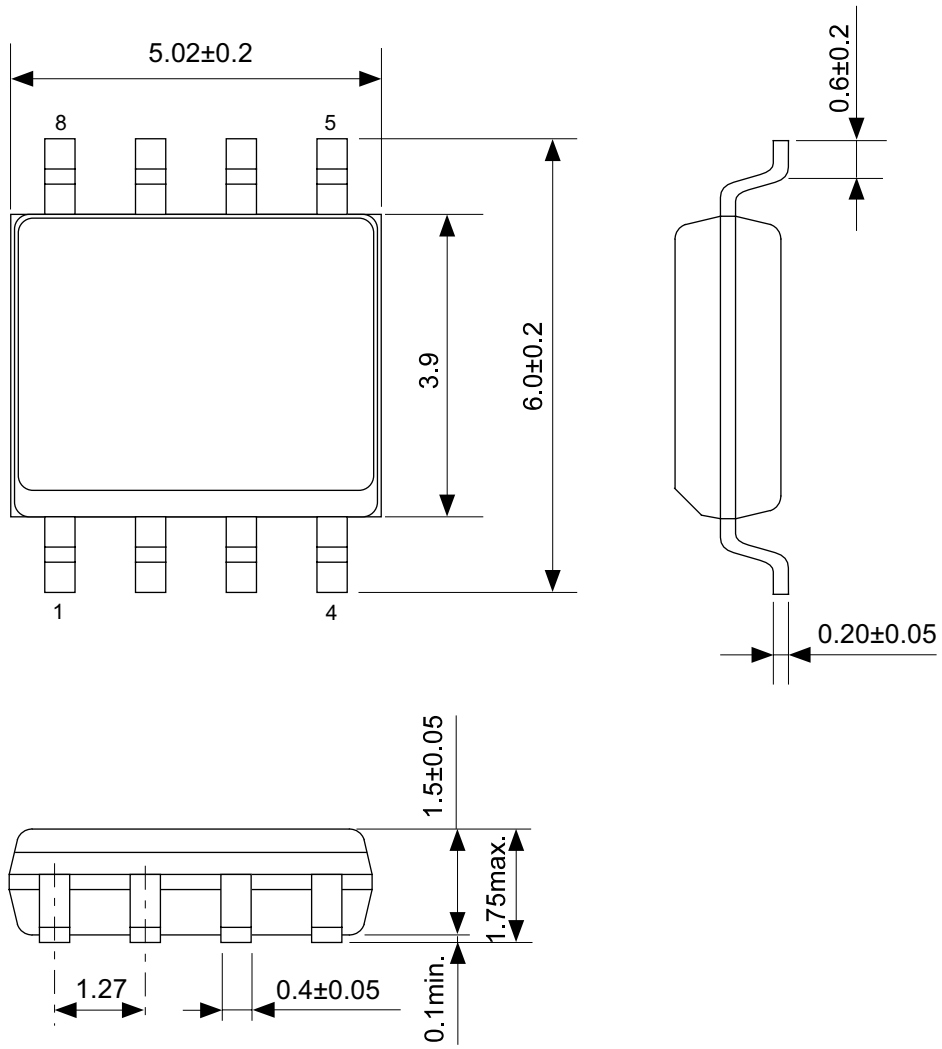
Operations with moisture on the E²PROM pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the E²PROM up from low temperature tank during the evaluation. Be sure that not remain frost on the E²PROM pin to prevent malfunction by short-circuit.
Also attention should be paid in using on environment, which is easy to dew for the same reason.

■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

■ Product Name Structure





No. FJ008-A-P-SD-2.1

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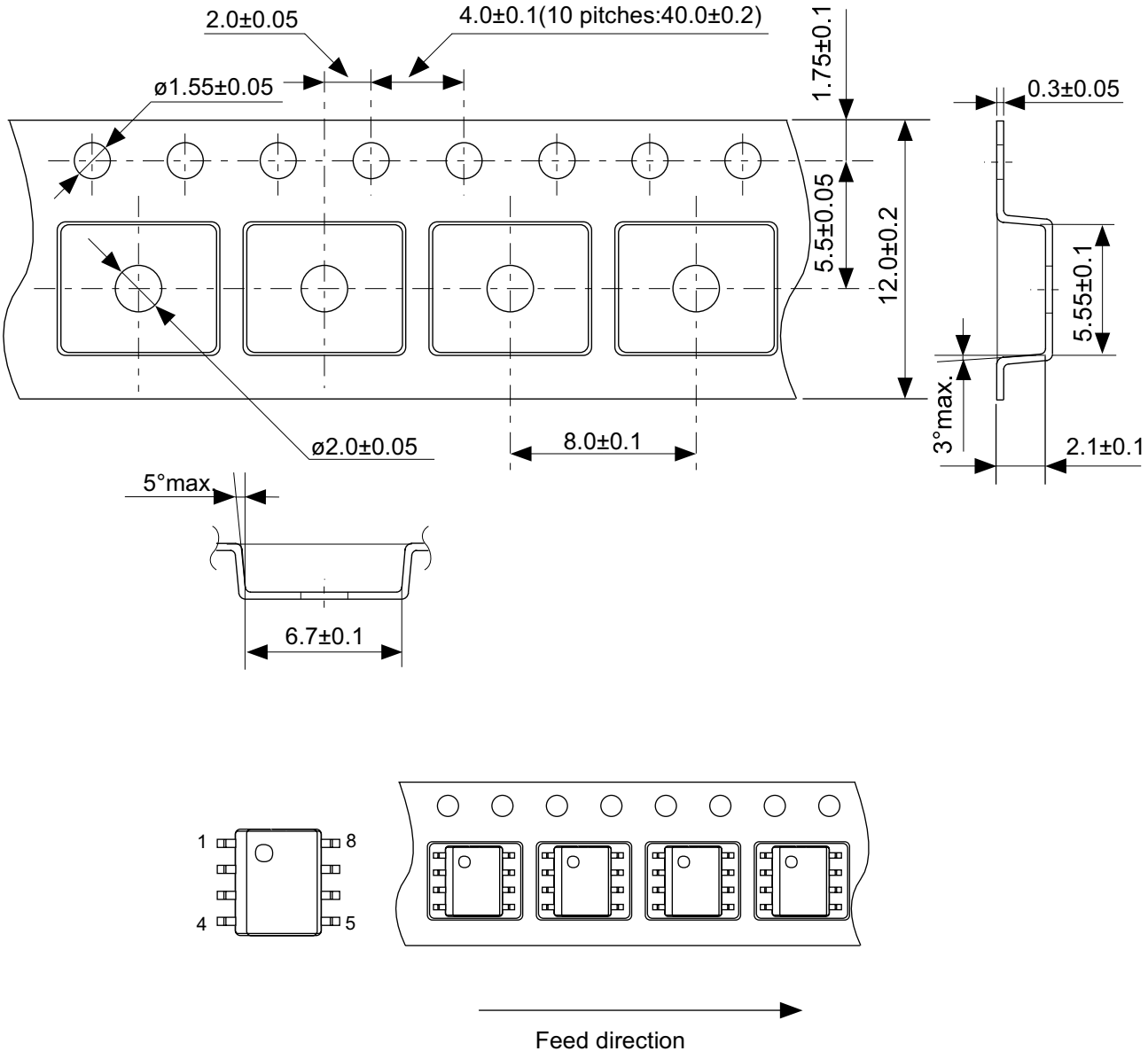
UNIT	mm
Seiko Instruments Inc.	



No. FJ008-D-C-SD-1.1

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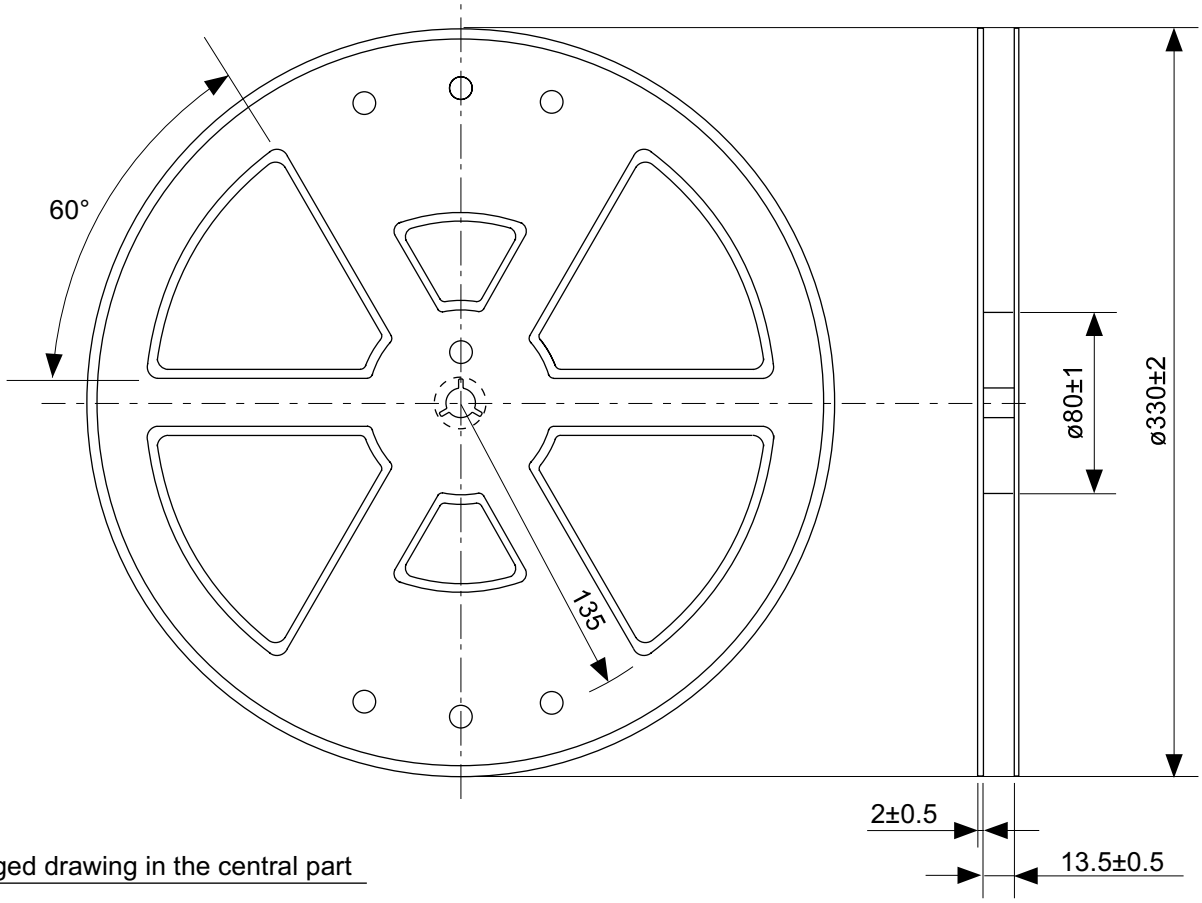
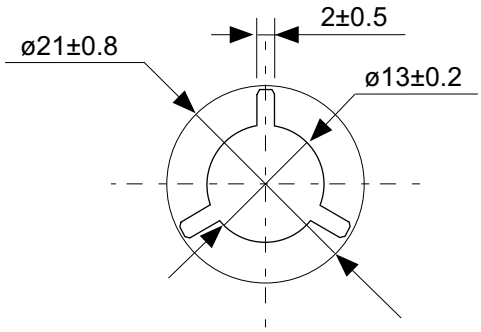
No.	FJ008-D-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FJ008-D-R-SD-1.1

TITLE	SOP8J-D-Reel		
No.	FJ008-D-R-SD-1.1		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			

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