

SN74CBTLV3257 低電圧、4ビット、1:2 FETマルチプレクサ/デマルチプレクサ

1 特長

- 2つのポート間を5Ωスイッチで接続
- データI/Oポートのレール・ツー・レール・スイッチング
- I_{off} により部分的パワーダウン・モードをサポート
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- JESD 22を超えるESD保護
 - 2000V、人体モデル(A114-A)
 - マシン・モデルで200V (A115-A)

2 アプリケーション

- モノのインターネット
- ワイヤレス・ヘッドフォン
- テレビジョン・セット
- 4ビット・バスの多重化および多重化解除

3 概要

SN74CBTLV3257デバイスは、4ビット、1:2の高速FETマルチプレクサおよびデマルチプレクサです。スイッチのON状態の抵抗が低いため、最小の伝播遅延で接続が可能です。

選択(S)入力により、データフローが制御されます。FETマルチプレクサ/デマルチプレクサは、出力イネーブル(\overline{OE})入力がHIGHのとき無効になります。

このデバイスは、 I_{off} を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。 I_{off} 機能により、パワーダウン時に損傷を引き起こすような電流がデバイスに逆流しないことが保証されます。デバイスは、電源オフ時は絶縁されています。

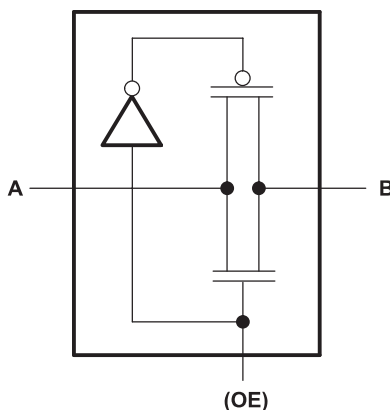
電源オンまたは電源オフ時に高インピーダンス状態を確保するため、 \overline{OE} はプルアップ抵抗経路で V_{CC} に接続します。この抵抗の最小値は、ドライバの電流シンク能力によって決定されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
SN74CBTLV3257DBQ	SSOP (16)	4.90mm×3.90mm
SN74CBTLV3257PW	TSSOP (16)	5.00mm×4.40mm
SN74CBTLV3257DGV	TVSOP (16)	3.60mm×4.40mm
SN74CBTLV3257D	SOIC (16)	9.90mm×3.91mm
SN74CBTLV3257RGY	VQFN (16)	4.00mm×3.50mm
SN74CBTLV3257RSV	UQFN (16)	2.60mm×1.80mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図(各FETスイッチ)



目次

1	特長	1	8.4	Device Functional Modes	8
2	アプリケーション	1	9	Application and Implementation	9
3	概要	1	9.1	Application Information	9
4	改訂履歴	2	9.2	Typical Application	9
5	Pin Configuration and Functions	3	10	Power Supply Recommendations	10
6	Specifications	5	11	Layout	11
6.1	Absolute Maximum Ratings	5	11.1	Layout Guidelines	11
6.2	ESD Ratings	5	11.2	Layout Example	11
6.3	Recommended Operating Conditions	5	12	デバイスおよびドキュメントのサポート	12
6.4	Thermal Information	5	12.1	ドキュメントのサポート	12
6.5	Electrical Characteristics	6	12.2	ドキュメントの更新通知を受け取る方法	12
6.6	Switching Characteristics	6	12.3	コミュニティ・リソース	12
7	Parameter Measurement Information	7	12.4	商標	12
8	Detailed Description	8	12.5	静電気放電に関する注意事項	12
8.1	Overview	8	12.6	Glossary	12
8.2	Functional Block Diagram	8	13	メカニカル、パッケージ、および注文情報	12
8.3	Feature Description	8			

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision L (October 2016) から Revision M に変更	Page
• Changed the pin images appearance	3
• Changed the <i>Thermal Information</i> table	5

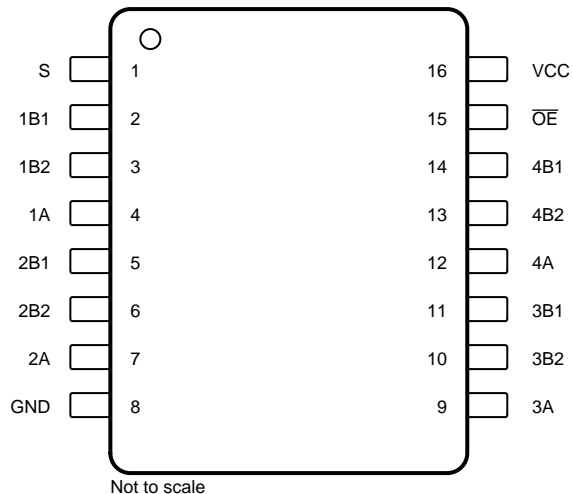
Revision K (April 2015) から Revision L に変更	Page
• 「製品情報」表にTSSOP (16)を 追加	1
• Added Junction temperature, T_J in <i>Absolute Maximum Ratings</i>	5
• Changed wording in <i>Detailed Design Procedure</i> to clarify device operation	10
• 追加「ドキュメントの更新通知を受け取る方法」セクションおよび「コミュニティ・リソース」セクション	12

Revision J (December 2012) から Revision K に変更	Page
• 「注文情報」表を削除、「メカニカル、パッケージ、および注文情報」を参照	1
• 「ピン構成および機能」セクション、「ESD定格」セクション、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクション 追加	1
• 「アプリケーション」追加	1
• 「製品情報」表 追加	1

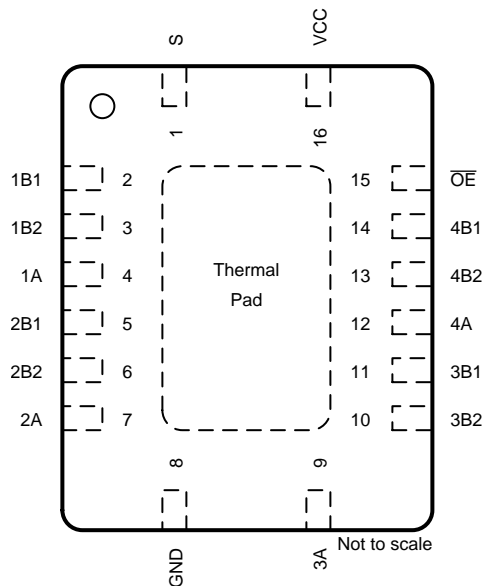
Revision I (October 2003) から Revision J に変更	Page
• QFN注文情報とパッケージのピン配置を追加	1

5 Pin Configuration and Functions

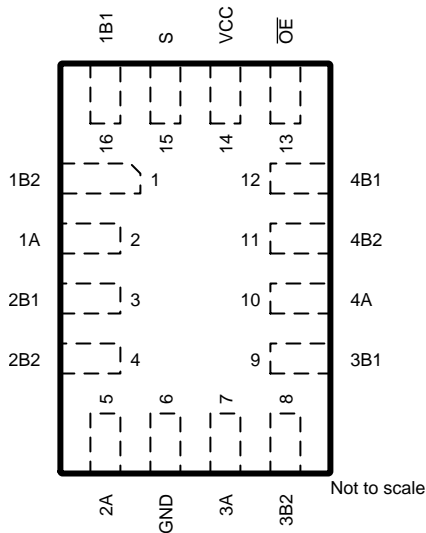
**D, DBQ, DGV, and PW Package
16-Pin SOIC, SSOP, TVSOP, and TSSOP
(Top View)**



**RGY Package
16-Pin VQFN
(Top View)**



**RSV Package
16-Pin UQFN
(Top View)**



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOIC, SSOP, TVSOP, TSSOP, VQFN	UQFN		
1A	4	2	I/O	Channel 1 out/in common
1B1	2	16	I/O	Channel 1 in/out 1
1B2	3	1	I/O	Channel 1 in/out 2
2A	7	5	I/O	Channel 2 out/in common
2B1	5	3	I/O	Channel 2 in/out 1
2B2	6	4	I/O	Channel 2 in/out 2
3A	9	7	I/O	Channel 3 out/in common
3B1	11	9	I/O	Channel 3 in/out 1
3B2	10	8	I/O	Channel 3 in/out 2
4A	12	10	I/O	Channel 4 out/in common
4B1	14	12	I/O	Channel 4 in/out 1
4B2	13	11	I/O	Channel 4 in/out 2
GND	8	6	—	Ground
\overline{OE}	15	13	I	Output Enable, active low
S	1	15	I	Select
V _{CC}	16	14	—	Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	4.6	V
V _I	Input voltage ⁽²⁾	-0.5	4.6	V
	Continuous channel current		128	mA
I _{IK}	Input clamp current	V _{I/O} < 0	-50	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V V _{CC} = 2.7 V to 3.6 V	1.7 2	V
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V V _{CC} = 2.7 V to 3.6 V	0.7 0.8	V
T _A	Operating free-air temperature	-40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#) SCBA004.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74CBTLV3257					UNIT	
	D	DBQ	DGV	PW	RGY		
	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	86.7	112.4	123.1	110.9	43.8	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	47.8	63.6	48.7	45.8	57.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.7	54.8	54.9	56.0	21.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	12.3	17.0	5.2	5.4	1.7	°C/W
ψ _{JB}	Junction to board characterization parameter	43.5	54.4	54.3	55.4	21.5	°C/W
R _{θJC(botto m}	Junction-to-case (bottom) thermal resistance	-	-	-	-	9.7	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$, $I_I = -18\text{ mA}$				-1.2	V	
I_I		$V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}$ or GND				± 1	μA	
I_{off}		$V_{CC} = 0$, V_I or $V_O = 0$ to 3.6 V				15	μA	
I_{CC}		$V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND				10	μA	
ΔI_{CC} ⁽²⁾	Control inputs	$V_{CC} = 3.6\text{ V}$, One input at 3 V , Other inputs at V_{CC} or GND				300	μA	
C_i		$V_I = 3\text{ V}$ or 0				3	pF	
$C_{io(OFF)}$	A port	$V_O = 3\text{ V}$ or 0 , $\overline{OE} = V_{CC}$				10.5	pF	
	B port					5.5		
r_{on} ⁽³⁾	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$		$V_I = 0$	$I_I = 64\text{ mA}$	5	8	Ω	
				$I_I = 24\text{ mA}$	5	8		
	$V_I = 1.7\text{ V}$	$I_I = 15\text{ mA}$	27	40				
	$V_{CC} = 3\text{ V}$		$V_I = 0$	$I_I = 64\text{ mA}$	5	7		
				$I_I = 24\text{ mA}$	5	7		
			$V_I = 2.4\text{ V}$	$I_I = 15\text{ mA}$	10	15		

 (1) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

 (2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.

(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

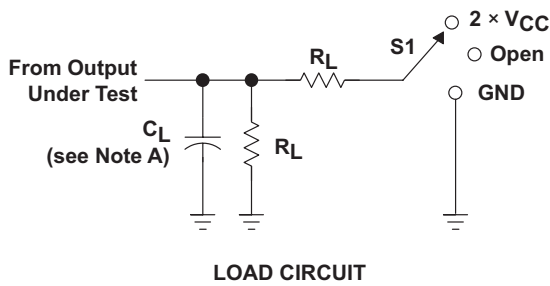
6.6 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (See [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5 \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B ⁽¹⁾	B or A	0.15		0.25		ns
	S	A or B	1.8	6.1	1.8	5.3	
t_{en}	S	A or B	1.7	6.1	1.7	5.3	ns
t_{dis}	S	A or B	1	4.8	1	4.5	ns
t_{en}	\overline{OE}	A or B	1.9	5.6	2	5	ns
t_{dis}	\overline{OE}	A or B	1	5.5	1.6	5.5	ns

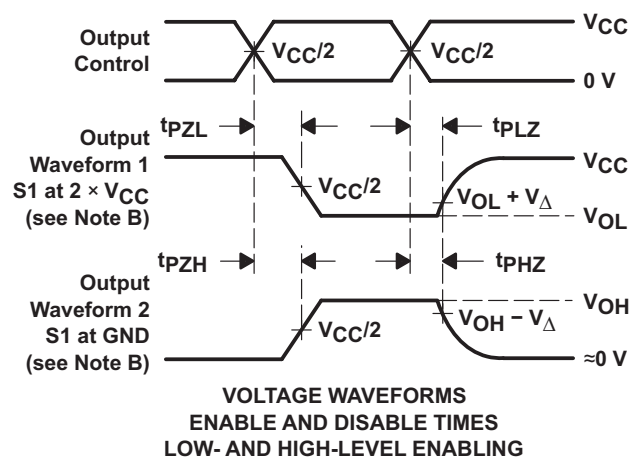
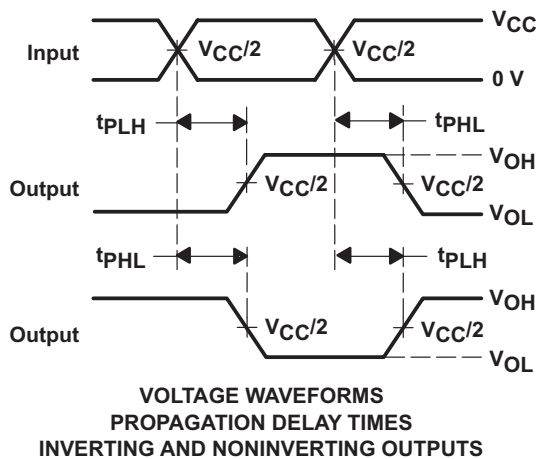
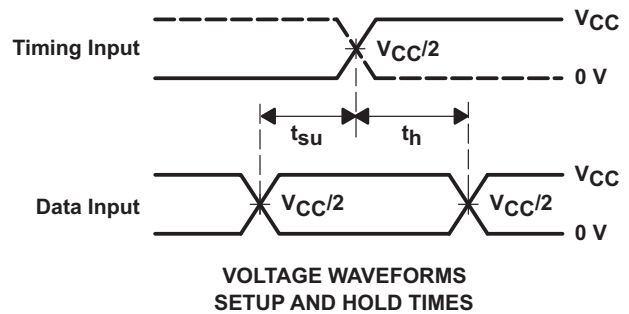
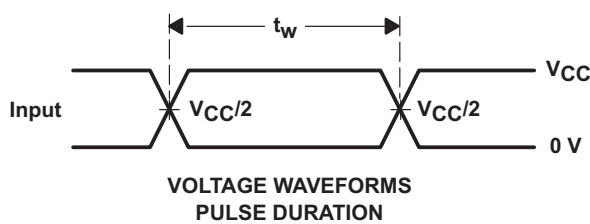
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

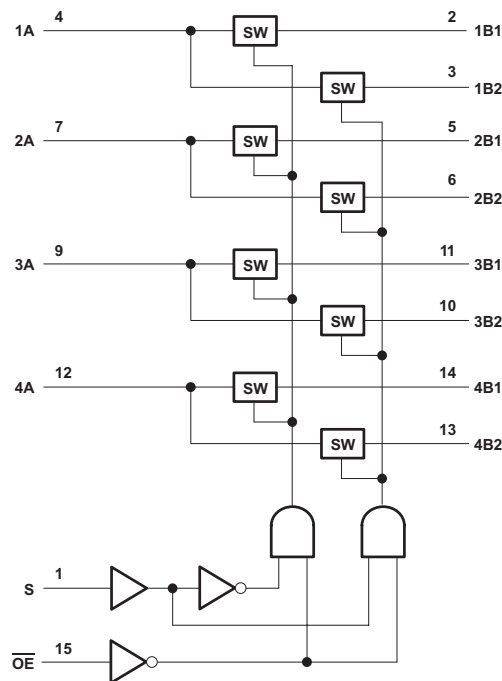
The SN74CBTLV3257 device is a 4-bit 1-of-2 high-speed FET multiplexer and demultiplexer. The low ON-state resistance of the switch allows connections to be made with minimal propagation delay.

The select (S) input controls the data flow. The FET multiplexers and demultiplexers are disabled when the output-enable (\overline{OE}) input is high.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram



8.3 Feature Description

The SN74CBTLV3257 features 5- Ω switch connection between ports, allowing for low signal loss across the switch. Rail-to-rail switching on data I/O allows for full voltage swing outputs. I_{off} supports partial-power-down mode operation, protecting the chip from voltages at output ports when it is not powered on. Latch-up performance exceeds 100 mA per JESD 78, Class II.

8.4 Device Functional Modes

Table 1 shows the functional modes of SN74CBTLV3257.

Table 1. Function Table

INPUTS		FUNCTION
\overline{OE}	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74CBTLV3257 can be used to multiplex and demultiplex up to 4 channels simultaneously in a 2:1 configuration. The application shown here is a 4-bit bus being multiplexed between two devices. The \overline{OE} and S pins are used to control the chip from the bus controller. This is a very generic example, and could apply to many situations. If an application requires less than 4 bits, be sure to tie the A side to either high or low on unused channels.

9.2 Typical Application

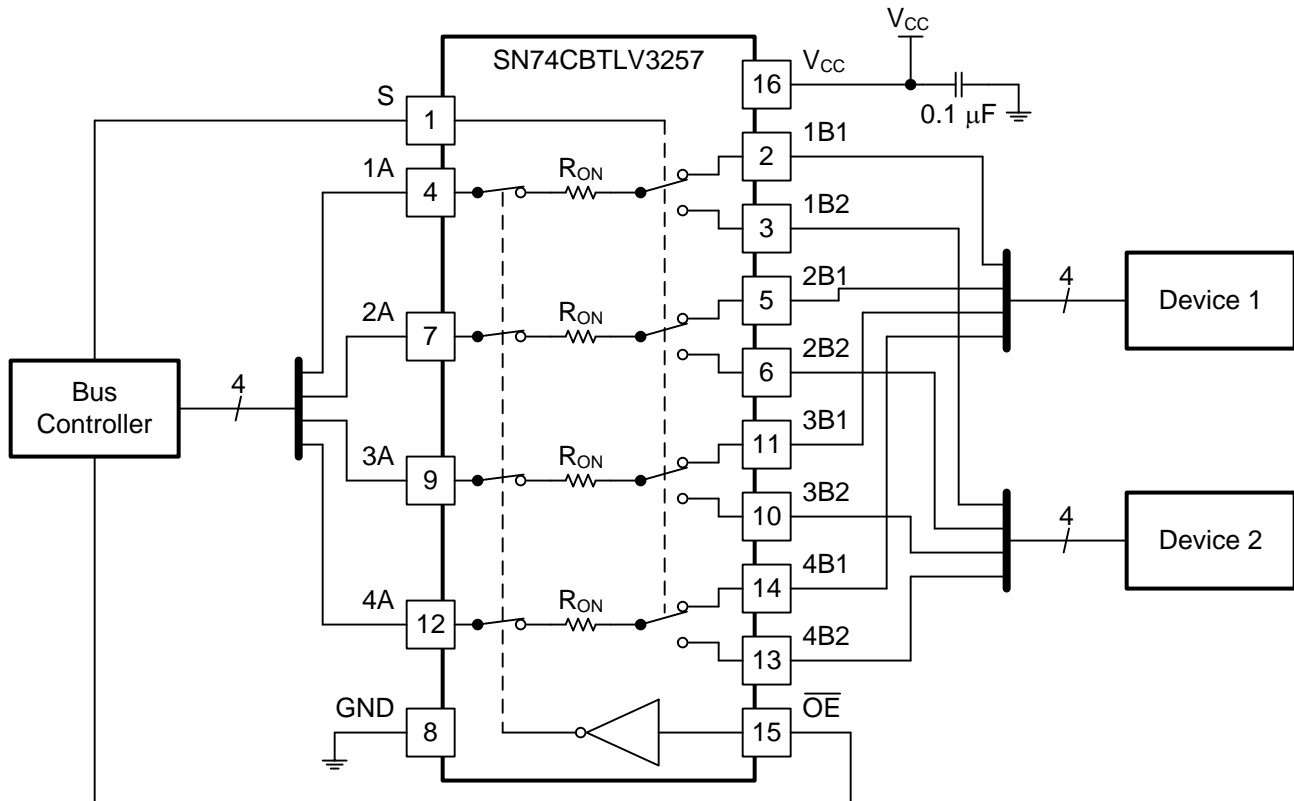


Figure 2. Typical Application of the SN74CBTLV3257

9.2.1 Design Requirements

1. Recommended Input Conditions:
 - For specified high and low levels, see V_{IH} and V_{IL} in [Recommended Operating Conditions](#).
 - Inputs and outputs are overvoltage tolerant allowing them to go as high as 4.6 V at any valid V_{CC} .
2. Recommended Output Conditions:
 - Load currents should not exceed ± 128 mA per channel.
3. Frequency Selection Criterion:
 - Maximum frequency tested is 200 MHz.

Typical Application (continued)

- Added trace resistance/capacitance can reduce maximum frequency capability; use layout practices as directed in [Layout](#).

9.2.2 Detailed Design Procedure

The 4-bit bus is connected directly to the 1A, 2A, 3A, and 4A ports (known as the xA port) on the SN74CBTLV3257, which essentially splits it into two busses, coming out of the xB1 and xB2 ports. When S is high, xB2 is the active bus, and when S is low, xB1 is the active bus. This means that Device 2 is connected to the bus controller when S is high, and Device 1 is connected to the bus controller when S is low. This setup is especially useful when two devices are hard coded with the same address and only one bus is available. The \overline{OE} connection can be used to disconnect all devices from the bus controller if necessary.

The 0.1- μ F capacitor on V_{CC} is a decoupling capacitor and should be placed as close as possible to the device.

9.2.3 Application Curve

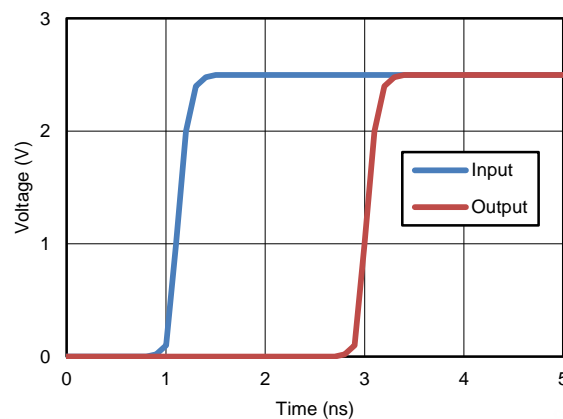


Figure 3. Propagation Delay (t_{pd}) Simulation Result at $V_{CC} = 2.5$ V

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating listed in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- μ F bypass capacitor is recommended. If multiple pins are labeled V_{CC} , then a 0.01- μ F or 0.022- μ F capacitor is recommended for each V_{CC} because the V_{CC} pins are tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD} , a 0.1- μ F bypass capacitor is recommended for each supply pin. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 μ F and 1 μ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to the loop antenna theory but are different enough to be discussed separately from the theory. When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

11.2 Layout Example

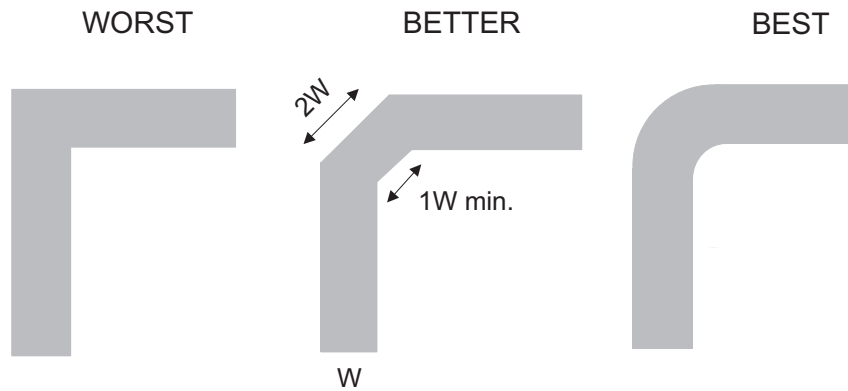


Figure 4. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- 『低速またはフローティングCMOS入力の影響』、SCBA004
- 『テキサス・インスツルメンツ製信号スイッチの的確な選択』、SZZA030

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74CBTLV3257PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
74CBTLV3257PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
74CBTLV3257RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
SN74CBTLV3257D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DBQR	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
SN74CBTLV3257DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CBTLV3257	Samples
SN74CBTLV3257PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	CL257	Samples
SN74CBTLV3257RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CL257	Samples
SN74CBTLV3257RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZTR	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

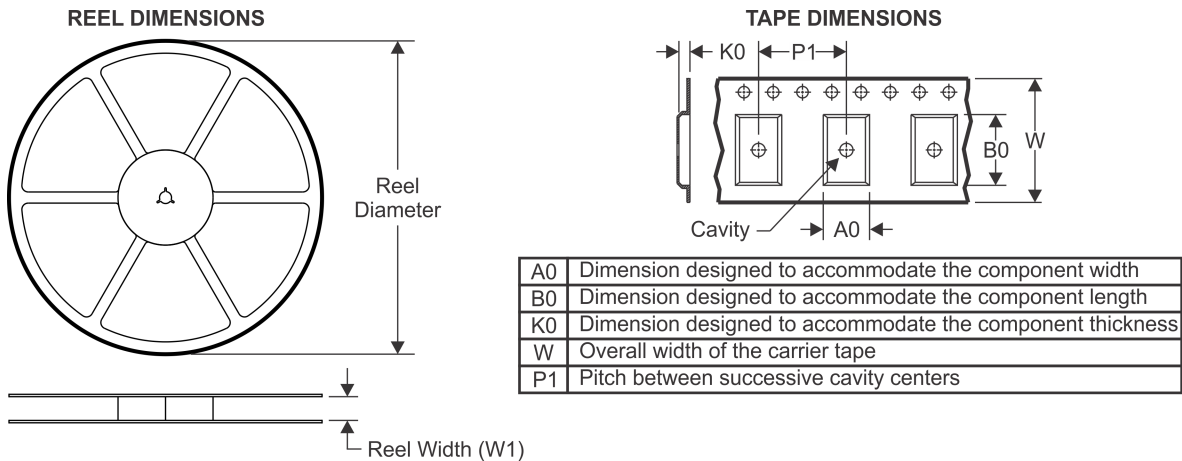
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTLV3257PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3257DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN74CBTLV3257DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74CBTLV3257DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74CBTLV3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3257PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74CBTLV3257RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74CBTLV3257RSVR	UQFN	RSV	16	3000	180.0	13.2	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTLV3257PWRG4	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CBTLV3257DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
SN74CBTLV3257DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74CBTLV3257DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74CBTLV3257PWR	TSSOP	PW	16	2000	364.0	364.0	27.0
SN74CBTLV3257PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74CBTLV3257RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
SN74CBTLV3257RSVR	UQFN	RSV	16	3000	180.0	180.0	30.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

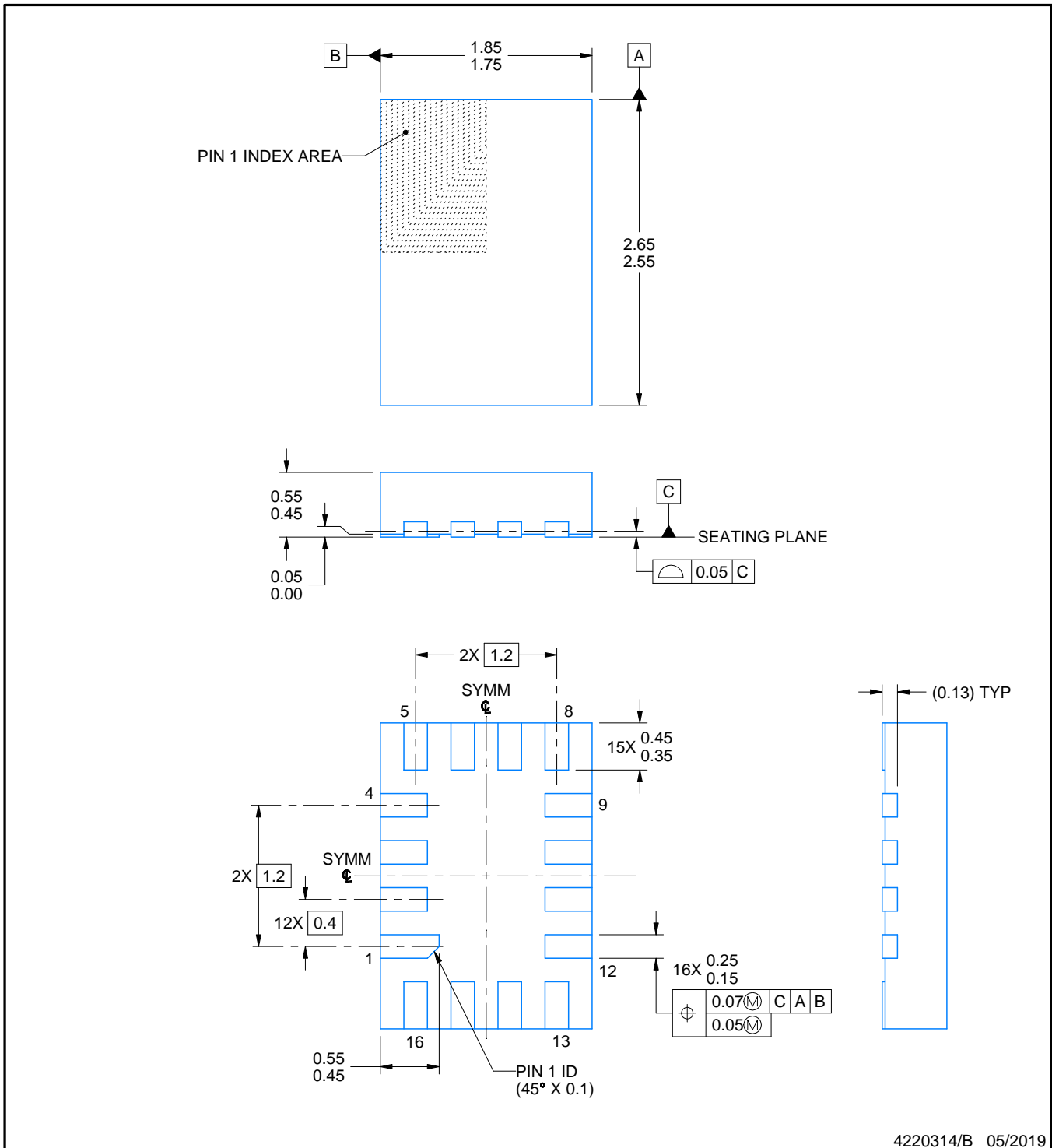
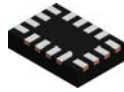


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4220314/B 05/2019

NOTES:

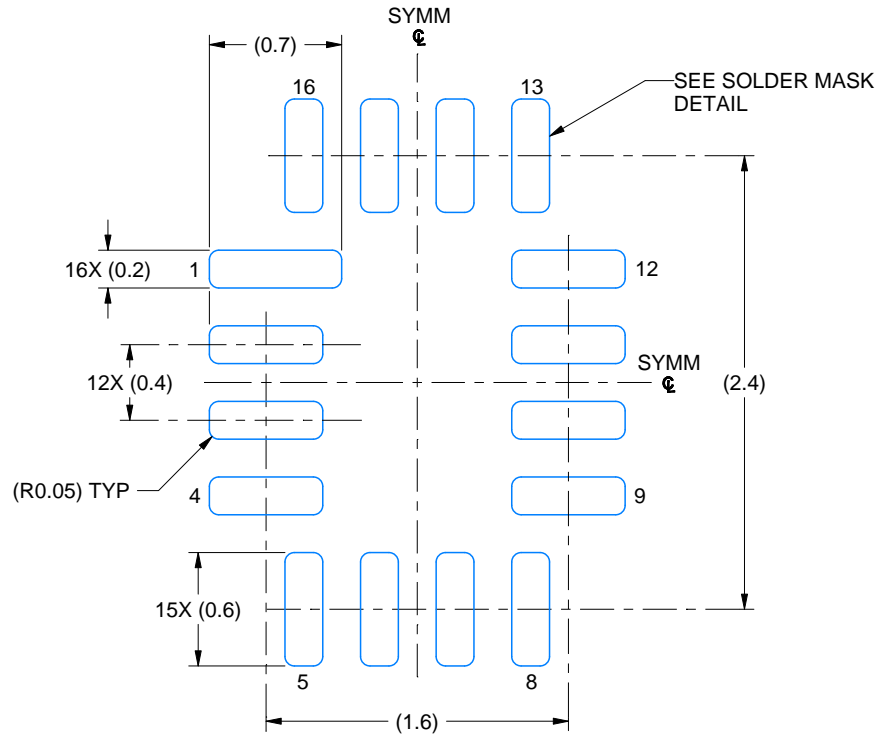
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

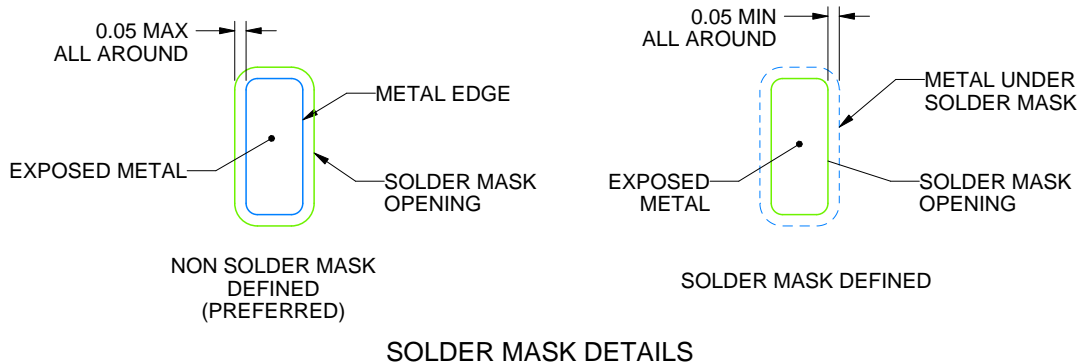
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4220314/B 05/2019

NOTES: (continued)

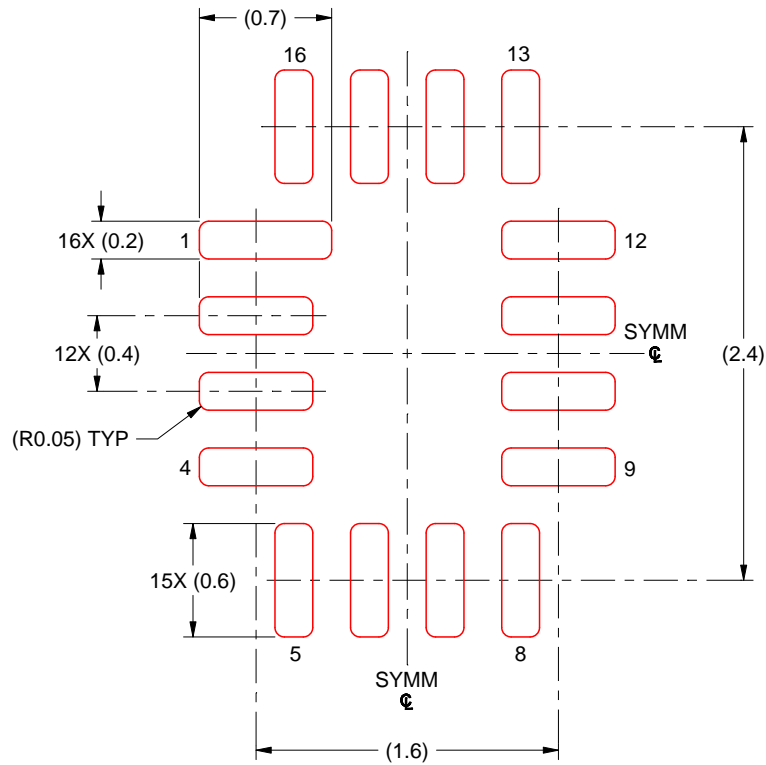
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/B 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



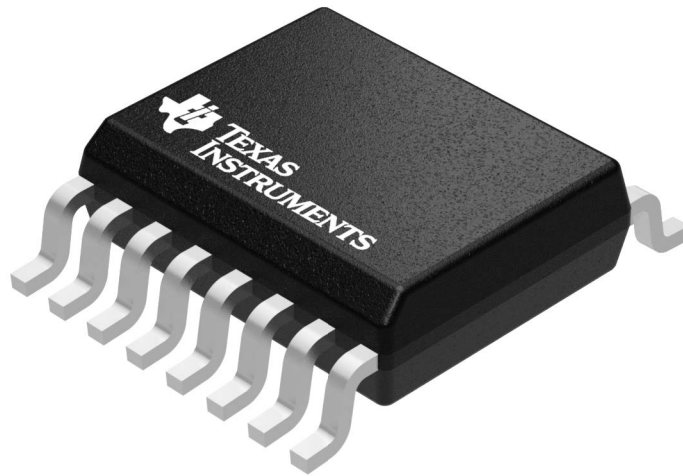
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

DBQ 16

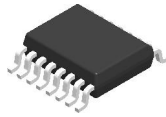
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4073301-2/1

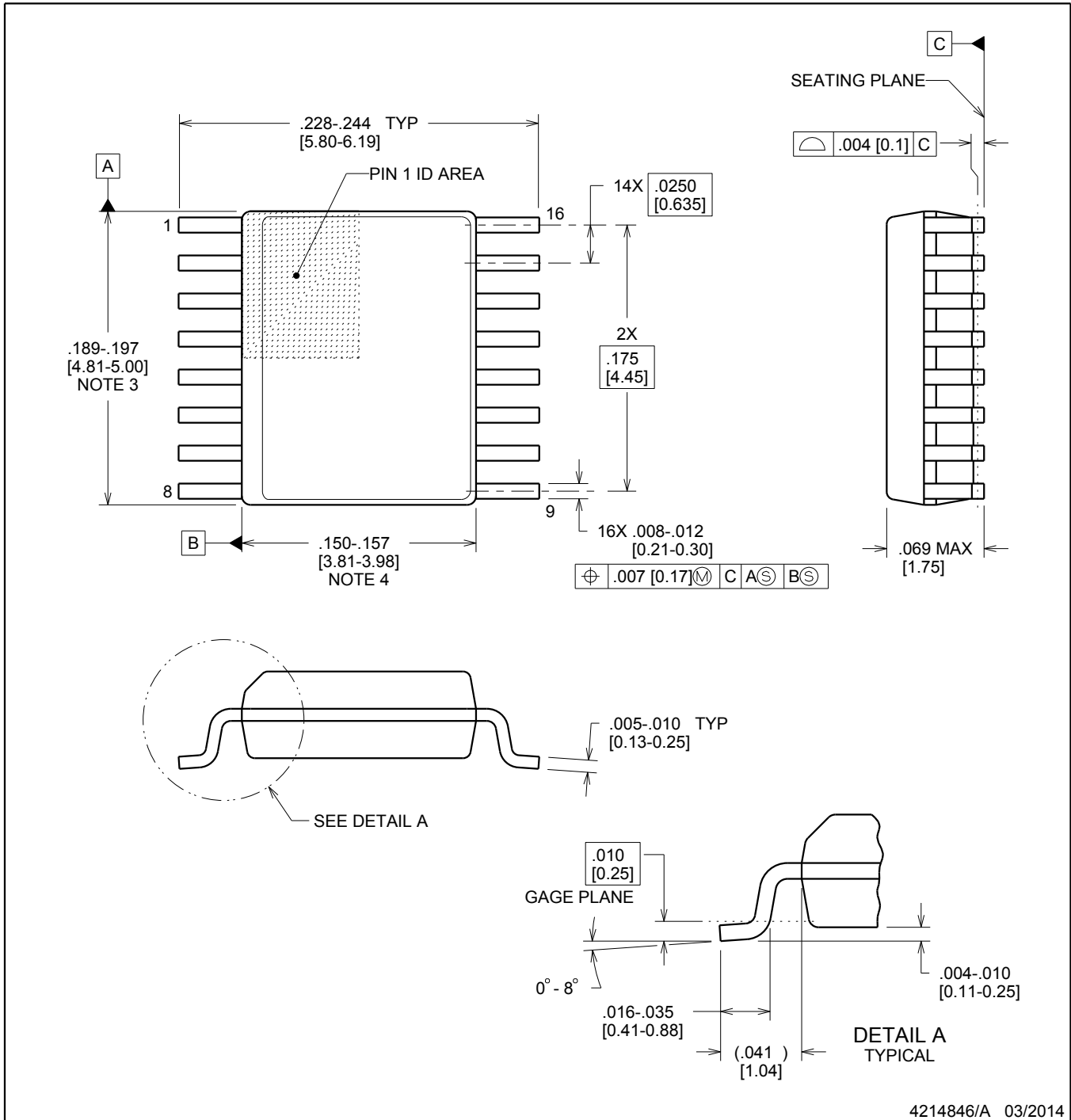


DBQ0016A

PACKAGE OUTLINE

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



4214846/A 03/2014

NOTES:

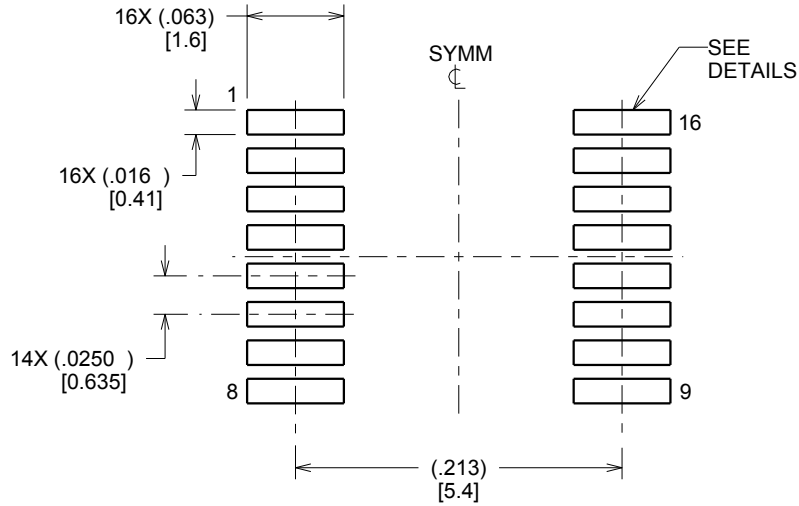
- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MO-137, variation AB.

EXAMPLE BOARD LAYOUT

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

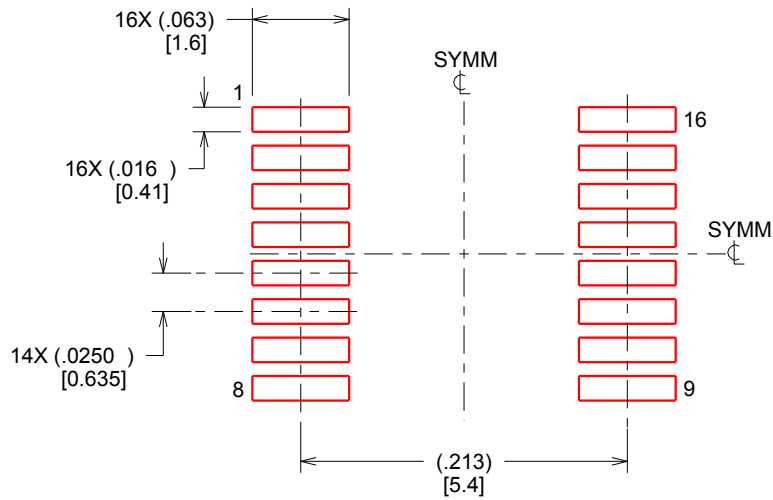
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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