



STP11NM80 - STF11NM80 STB11NM80 - STW11NM80

N-CHANNEL 800V - 0.35 Ω - 11 A TO-220 /FP/D²PAK/TO-247
MDmesh™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	R _{DS(on)} *Q _g	I _D
STP11NM80	800 V	< 0.40 Ω	14 Ω *nC	11 A
STF11NM80	800 V	< 0.40 Ω	14 Ω *nC	11 A
STB11NM80	800 V	< 0.40 Ω	14 Ω *nC	11 A
STW11NM80	800 V	< 0.40 Ω	14 Ω *nC	11 A

- TYPICAL R_{DS(on)} = 0.35 Ω
- LOW GATE INPUT RESISTANCE
- LOW INPUT CAPACITANCE AND GATE CHARGE
- BEST R_{DS(on)}*Q_g IN THE INDUSTRY

DESCRIPTION

The MDmesh™ associates the Multiple Drain process with the Company's PowerMesh™ horizontal layout assuring an outstanding low on-resistance. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competitor's products.

APPLICATIONS

The 800 V MDmesh™ family is very suitable for single switch applications in particular for Flyback and Forward converter topologies and for ignition circuits in the field of lighting.

Table 2: Order Codes

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP11NM80	P11NM80	TO-220	TUBE
STF11NM80	F11NM80	TO-220FP	TUBE
STB11NM80T4	B11NM80	D ² PAK	TAPE & REEL
STW11NM80	W11NM80	TO-247	TUBE

Figure 1: Package

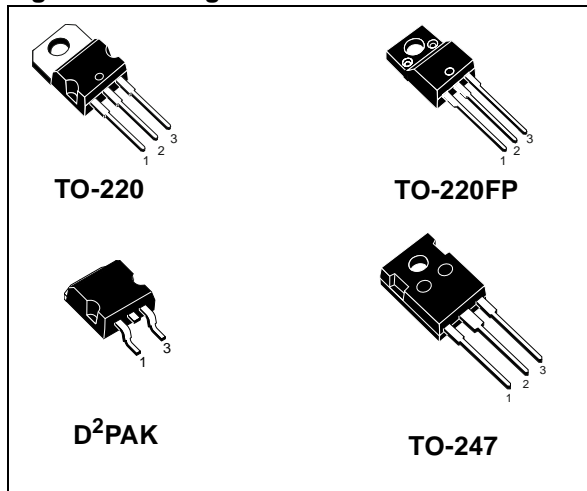


Figure 2: Internal Schematic Diagram

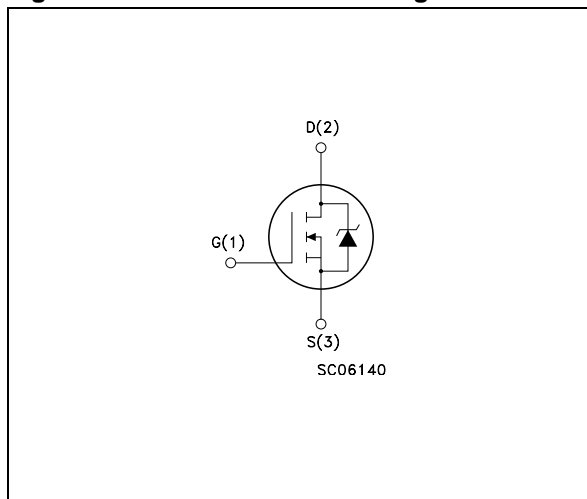


Table 3: Absolute Maximum ratings

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK TO-247	TO-220FP	
V _{DS}	Drain-source Voltage (V _{GS} = 0)	800		V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	800		V
V _{GS}	Gate- source Voltage	± 30		V
I _D	Drain Current (continuous) at T _C = 25°C	11	11 (*)	A
I _D	Drain Current (continuous) at T _C = 100°C	4.7	4.7 (*)	A
I _{DM} (•)	Drain Current (pulsed)	44	44 (*)	A
P _{TOT}	Total Dissipation at T _C = 25°C	150	35	W
	Derating Factor	1.2	0.28	W/°C
T _j T _{stg}	Operating Junction Temperature Storage Temperature	-65 to 150		°C

(•) Pulse width limited by safe operating area

(*) Limited only by the Maximum Temperature Allowed

Table 4: Thermal Data

		TO-220/D ² PAK TO-247	TO-220FP	Unit
R _{thj-case}	Thermal Resistance Junction-case Max	0.83	3.6	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	62.5		°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300		°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	2.5	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = 2.5A, V _{DD} = 50 V)	400	mJ

ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}C$ UNLESS OTHERWISE SPECIFIED)

Table 6: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	800			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			10 100	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 30V$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 5.5 A$		0.35	0.40	Ω

Table 7: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 7.5 A$		8		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz}, V_{GS} = 0$		1630 750 30		pF pF pF
R_G	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		2.7		Ω
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 400 V, I_D = 5.5 A$ $R_G = 4.7\Omega, V_{GS} = 10 V$ (Resistive Load see, Figure 4)		22 17 46 15		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 640 V, I_D = 11 A,$ $V_{GS} = 10V$		43.6 11.6 21		nC nC nC

Table 8: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				11 44	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 11 A, V_{GS} = 0$			0.86	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 11 A, di/dt = 100 A/\mu s$ $V_{DD} = 50 V, T_j = 25^{\circ}C$ (see test circuit, Figure 5)		612 7.22 23.6		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 11 A, di/dt = 100 A/\mu s$ $V_{DD} = 50 V, T_j = 150^{\circ}C$ (see test circuit, Figure 5)		970 11.25 23.2		ns μC A

Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Figure 3: Safe Operating Area For D²PAK/ TO-247 / TO-220

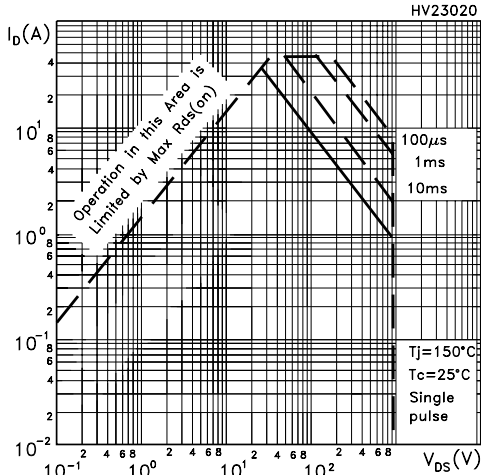


Figure 4: Thermal Impedance For D²PAK/ TO-247 / TO-220

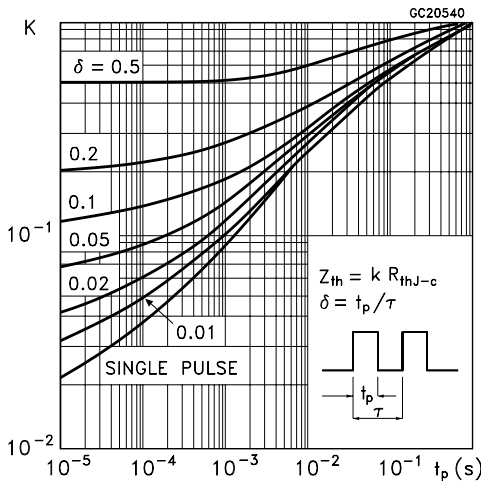


Figure 5: Output Characteristics

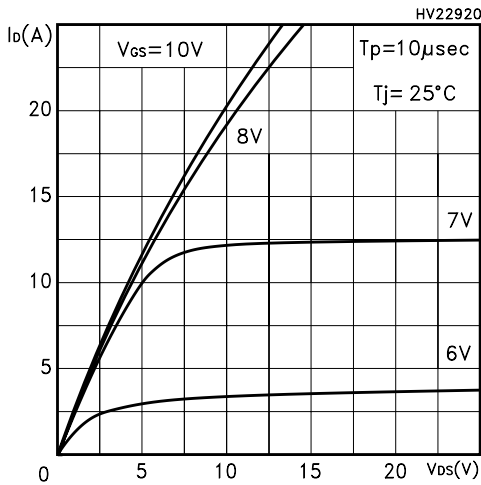


Figure 6: Safe Operating Area For TO-220FP

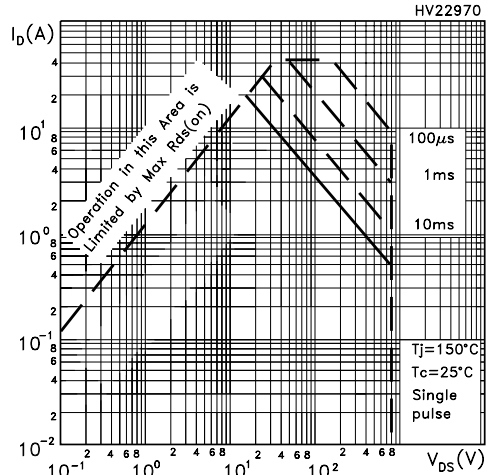


Figure 7: Thermal Impedance For TO-220FP

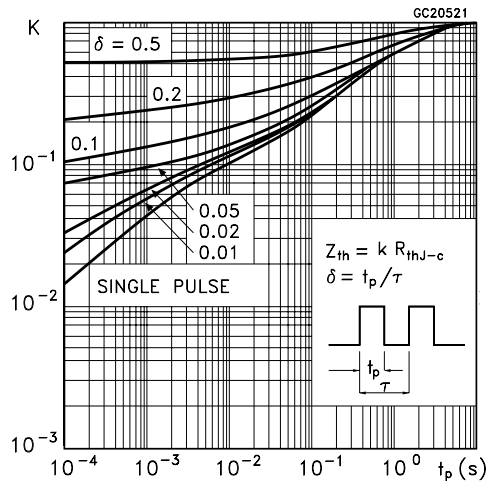


Figure 8: Output Characteristics

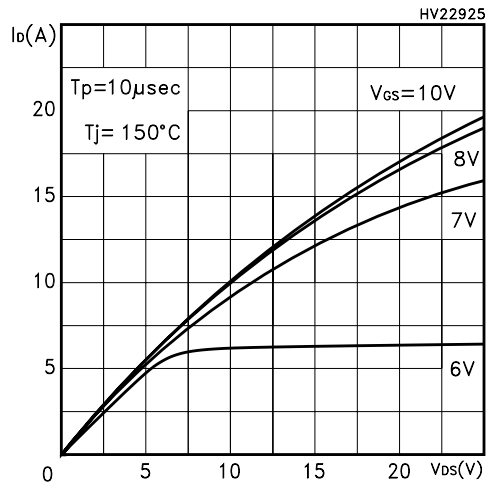


Figure 9: Transfer Characteristics

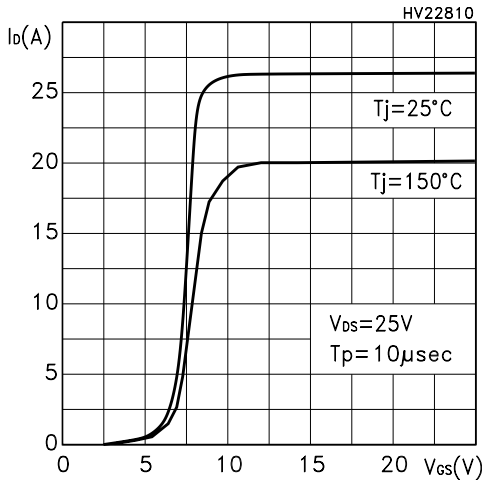


Figure 10: Transconductance

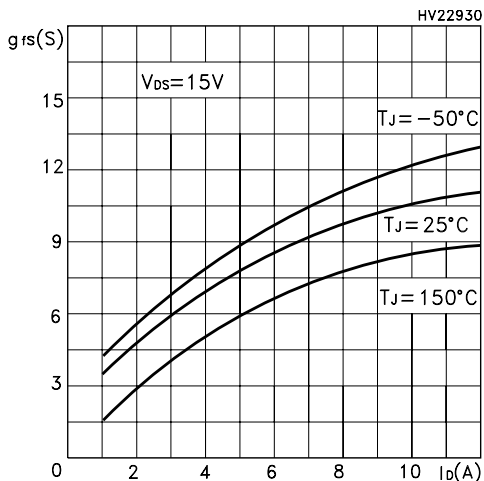


Figure 11: Gate Charge vs Gate-source Voltage

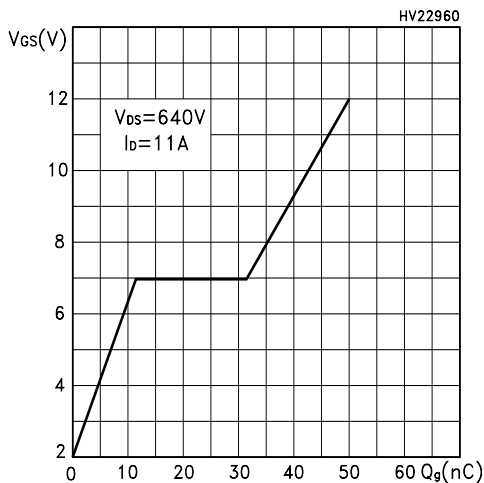


Figure 12: Normalized Gate Threshold Voltage vs Temperature

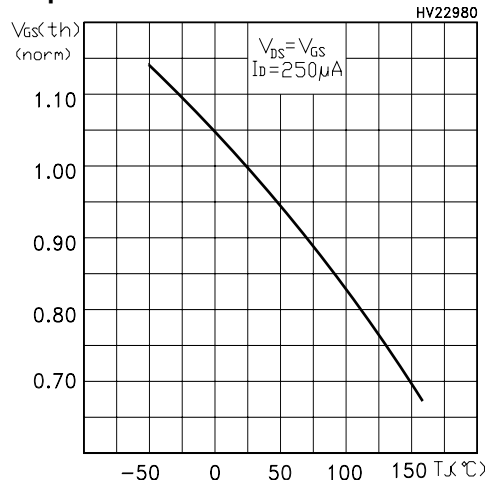


Figure 13: Static Drain-Source On Resistance

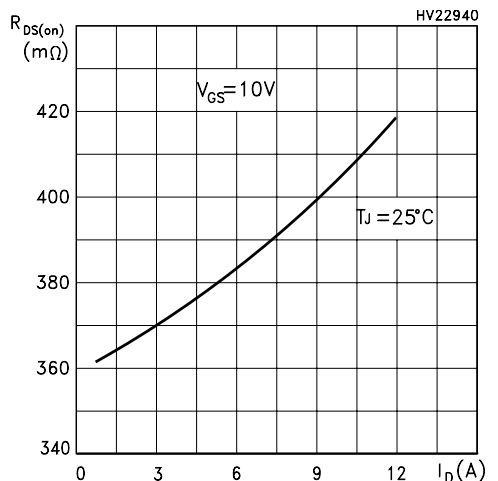


Figure 14: Capacitance Variations

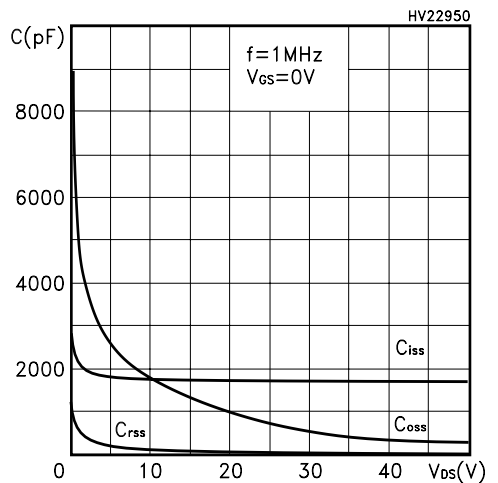


Figure 15: Normalized On Resistance vs Temperature

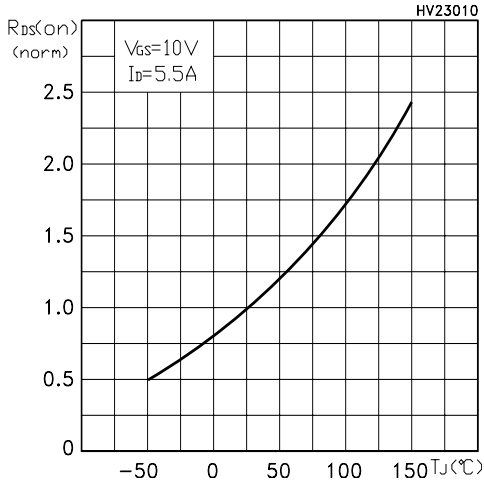


Figure 17: Normalized BV_{DSS} vs Temperature

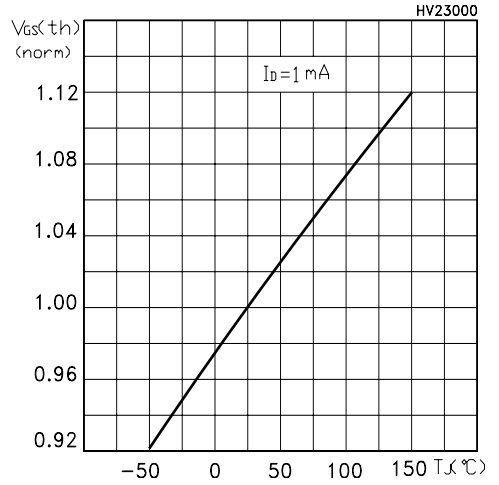


Figure 16: Source-Drain Forward Characteristics

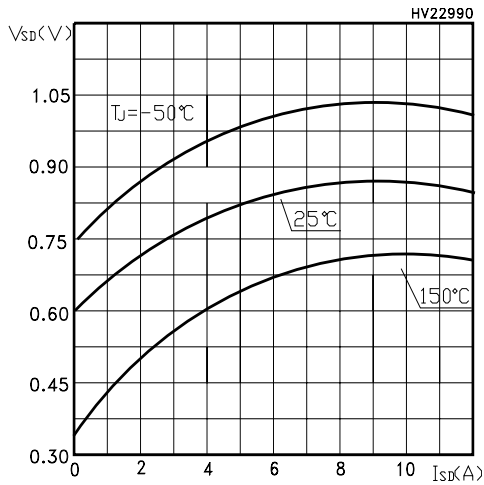


Figure 18: Unclamped Inductive Load Test Circuit



Figure 19: Switching Times Test Circuit For Resistive Load



Figure 20: Test Circuit For Inductive Load Switching and Diode Recovery Times

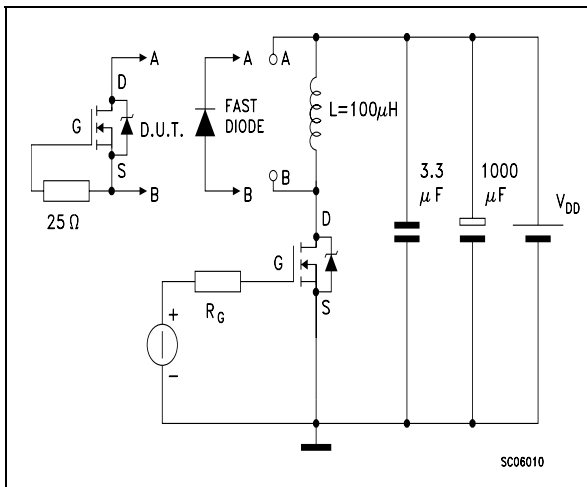


Figure 21: Unclamped Inductive Waferform

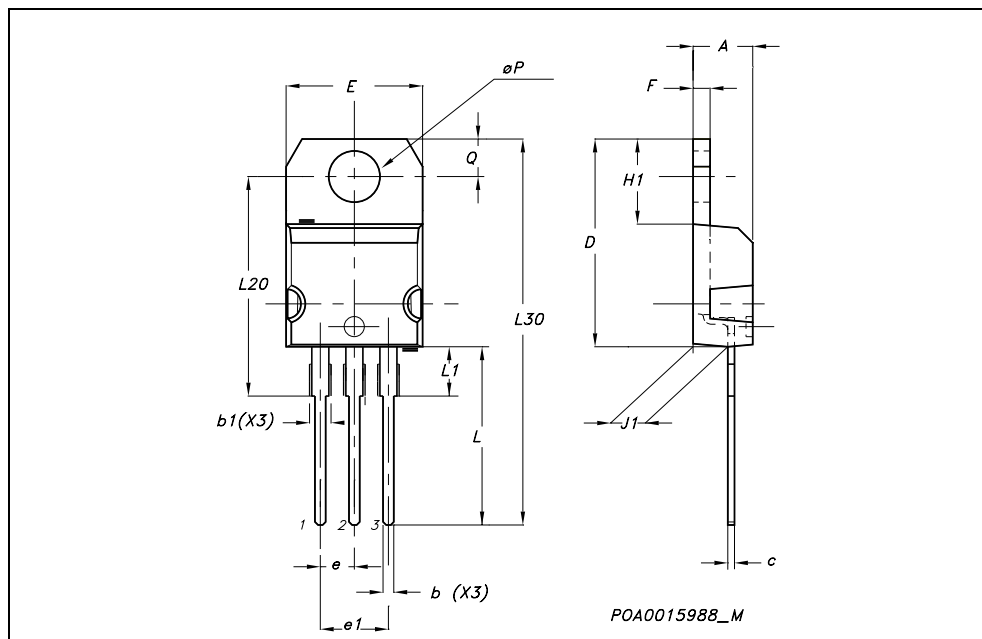


Figure 22: Gate Charge Test Circuit



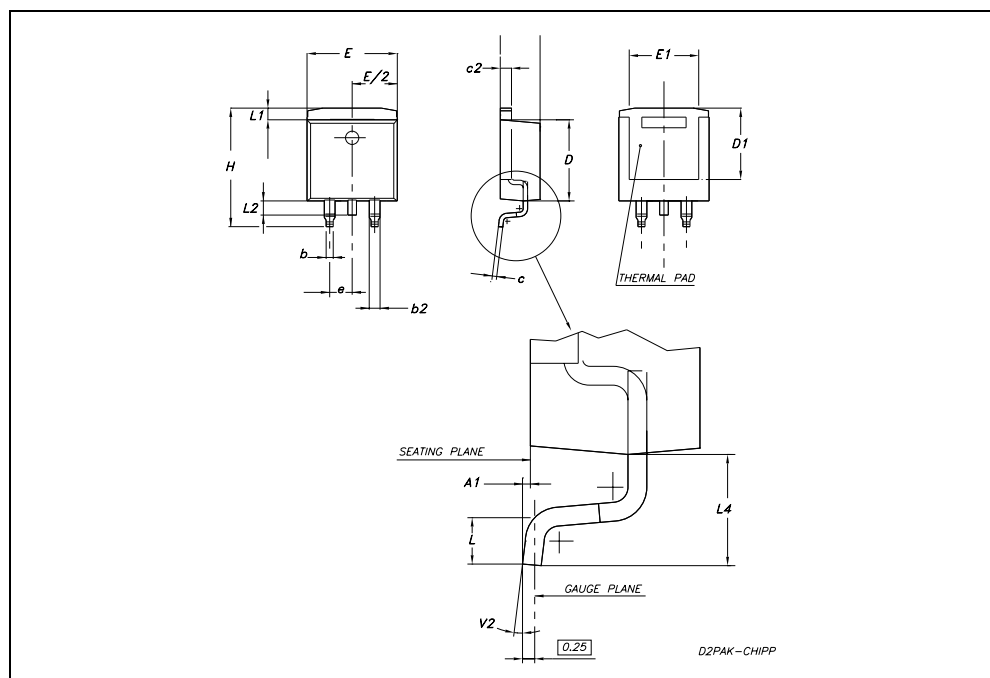
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



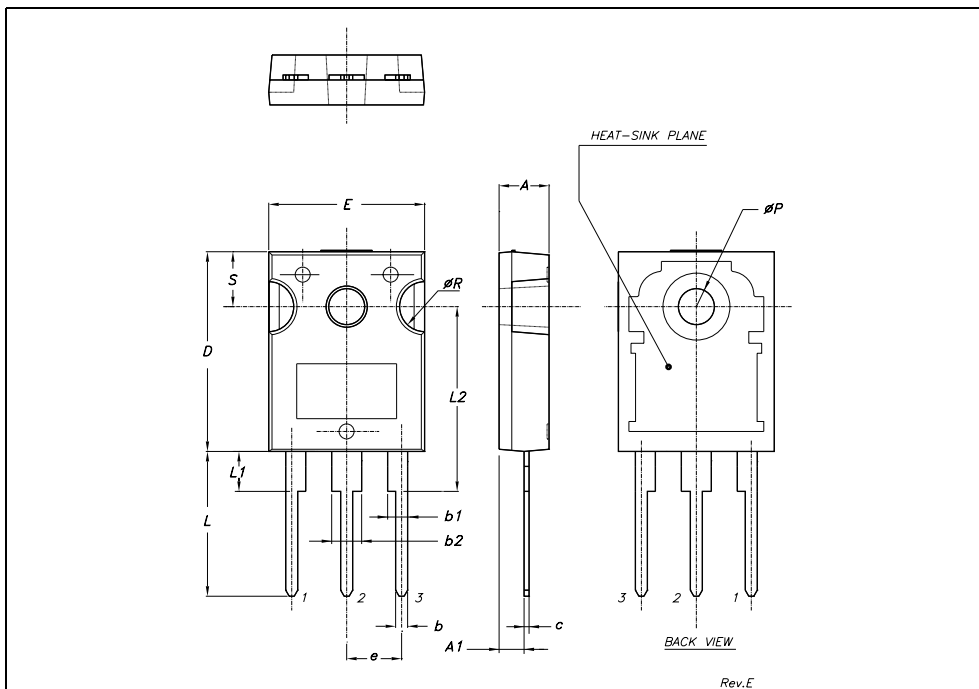
TO-263 (D²PAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.32		4.57	0.178		0.180
A1	0.00		0.25	0.00		0.009
b	0.71		0.91	0.028		0.350
b2	1.15		1.40	0.045		0.055
c	0.46		0.61	0.018		0.024
c2	1.22		1.40	0.048		0.055
D	8.89	9.02	9.40	0.350	0.355	0.370
D1	8.01			0.315		
E	10.04		10.28	0.395		0.404
e		2.54			0.010	
H	13.10		13.70	0.515		0.540
L	1.30		1.70	0.051		0.067
L1	1.15		1.39	0.045		0.054
L2	1.27		1.77	0.050		0.069
L4	2.70		3.10	0.106		0.122
V2	0°		8°	0°		8°

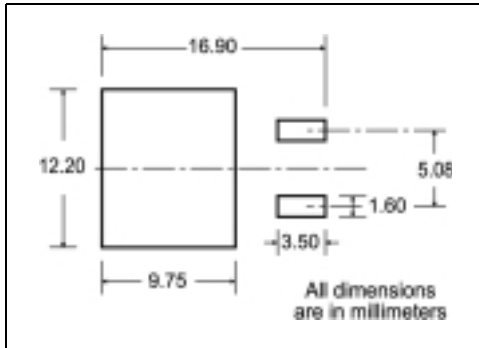


TO-247 MECHANICAL DATA

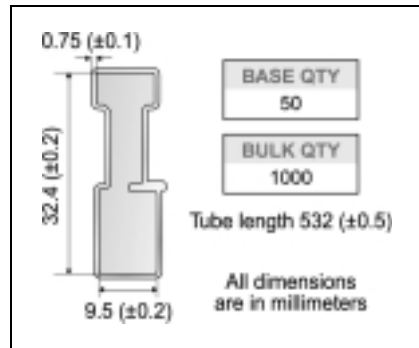
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

* on sales type

Figure 23: Revision History

Date	Revision	Description of Changes
29-Jul-2004	1	Final Document

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