

SWITCHING  
DUAL N-CHANNEL POWER MOS FET  
INDUSTRIAL USE

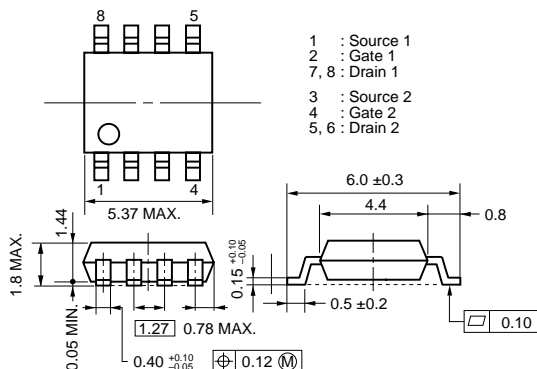
DESCRIPTION

The  $\mu$ PA1763 is N-Channel MOS Field Effect Transistor designed for DC/DC Converters.

FEATURES

- Dual chip type
- Low on-resistance
- ★  $R_{DS(on)1} = 47.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2.3 \text{ A)}$
- ★  $R_{DS(on)2} = 57.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 2.3 \text{ A)}$
- ★  $R_{DS(on)3} = 66.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 2.3 \text{ A)}$
- Low input capacitance
- ★  $C_{iss} = 870 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



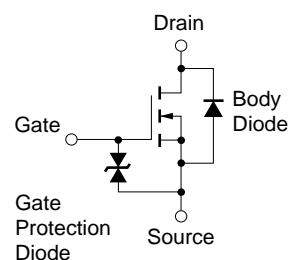
ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA1763G	Power SOP8

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25 \text{ }^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 4.5$	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	$\pm 18$	A
Total Power Dissipation (1 unit) <sup>Note2</sup>	$P_T$	1.7	W
Total Power Dissipation (2 unit) <sup>Note2</sup>	$P_T$	2.0	W
★ Single Avalanche Current <sup>Note3</sup>	$I_{AS}$	4.5	A
★ Single Avalanche Energy <sup>Note3</sup>	$E_{AS}$	60	mJ
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$

EQUIVALENT CIRCUIT  
(1/2 Circuit)



- Notes
1.  $PW \leq 10 \text{ } \mu\text{s}$ , Duty cycle  $\leq 1 \%$
  2.  $T_A = 25 \text{ }^\circ\text{C}$ , Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
  - ★ 3. Starting  $T_{ch} = 25 \text{ }^\circ\text{C}$ ,  $R_G = 25 \text{ } \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

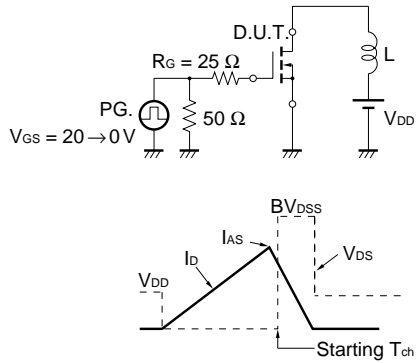
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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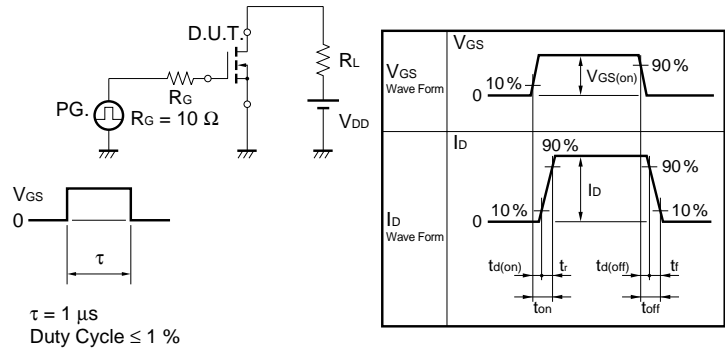
★ ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.3 A		37.0	47.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 2.3 A		45.0	57.0	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 2.3 A		49.0	66.0	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.3 A	3.0	6.0		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iSS</sub>	V <sub>DS</sub> = 10 V		870		pF
Output Capacitance	C <sub>oSS</sub>	V <sub>GS</sub> = 0 V		150		pF
Reverse Transfer Capacitance	C <sub>rSS</sub>	f = 1 MHz		80		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 2.3 A		11		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 10 V		40		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 30 V		50		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		12		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 4.5 A		20		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 48 V		3		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		5		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 4.5 A, V <sub>GS</sub> = 0 V		0.80		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 4.5 A, V <sub>GS</sub> = 0 V		30		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		40		nC

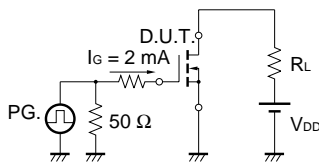
TEST CIRCUIT 1 AVALANCHE CAPABILITY



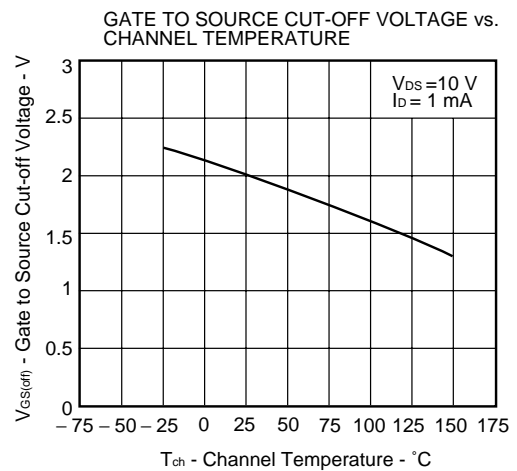
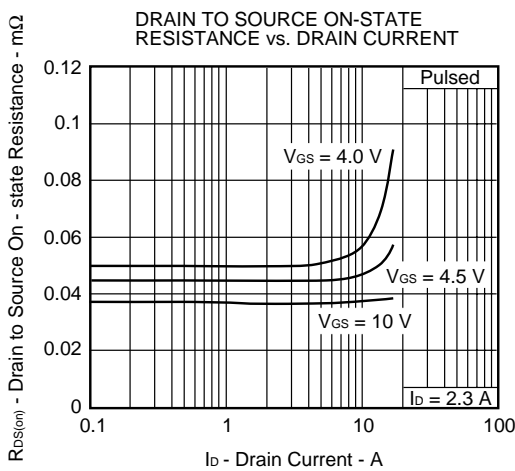
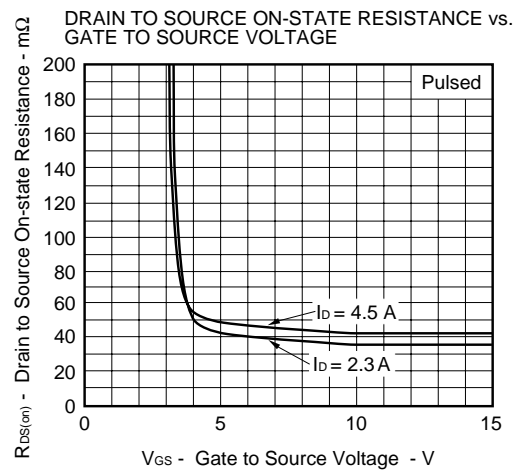
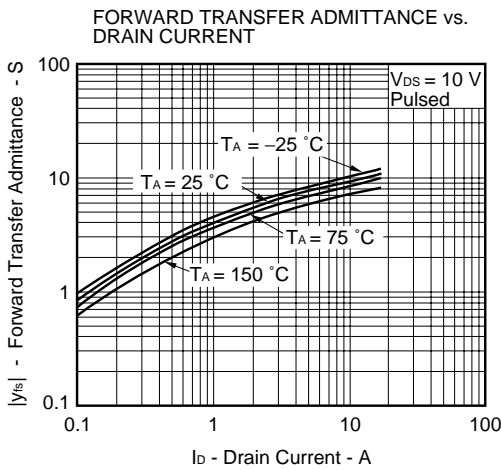
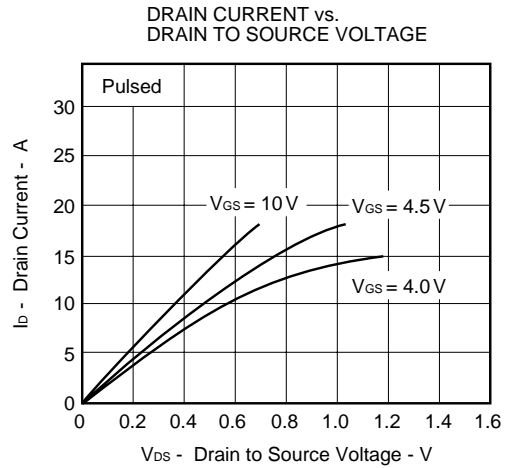
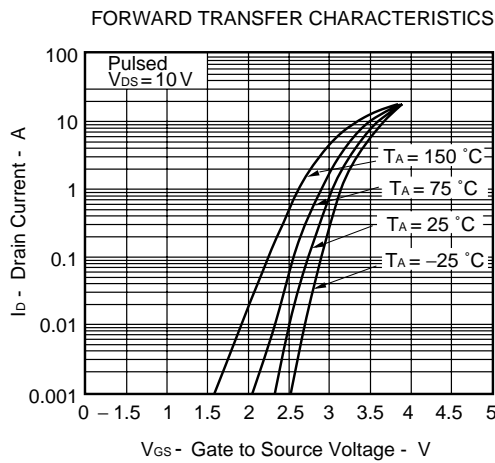
TEST CIRCUIT 2 SWITCHING TIME



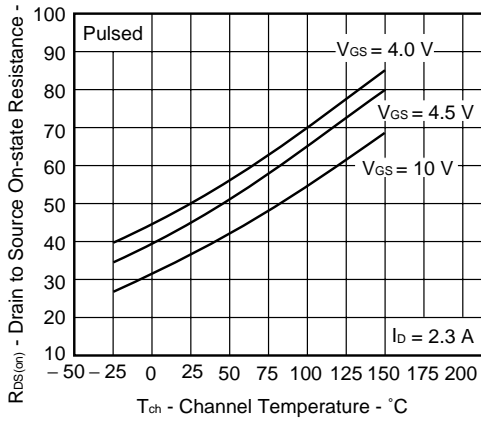
★ TEST CIRCUIT 3 GATE CHARGE



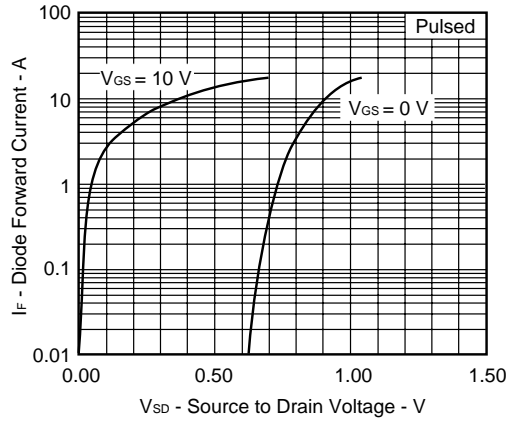
★ TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)



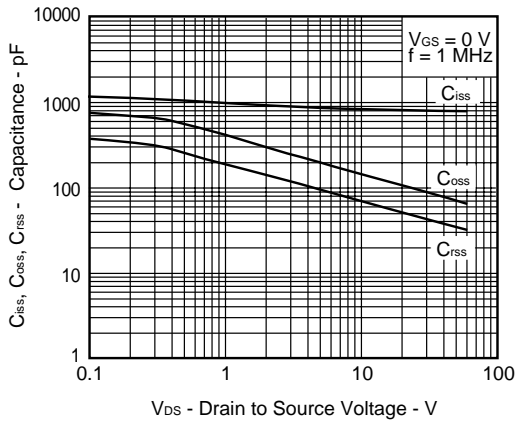
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



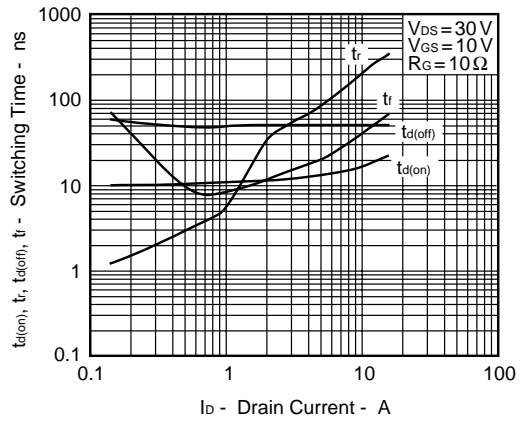
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



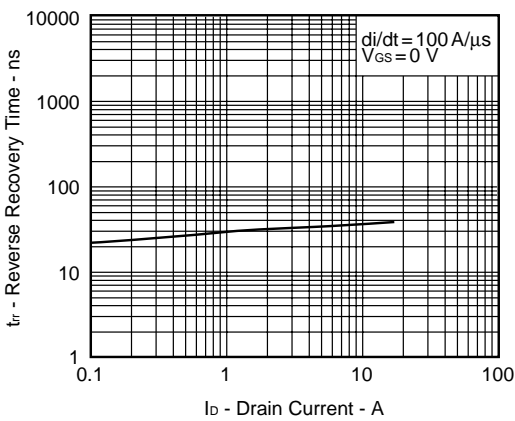
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



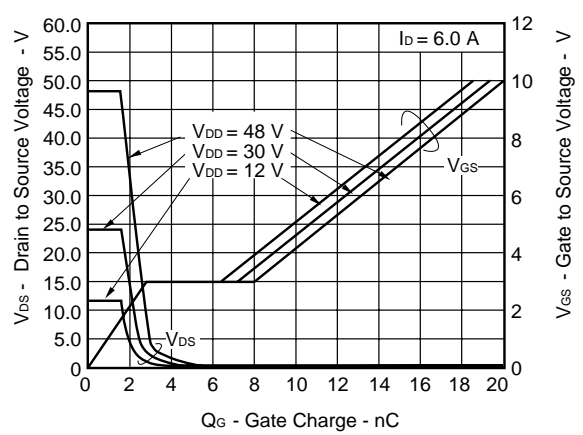
SWITCHING CHARACTERISTICS



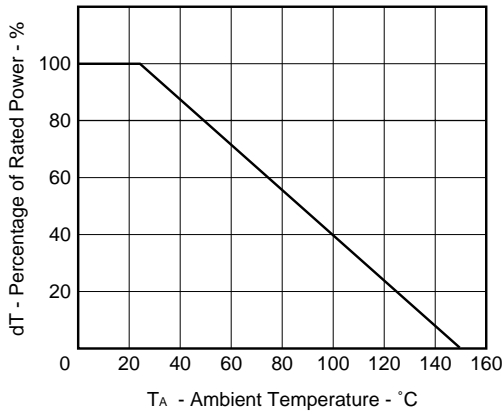
REVERSE RECOVERY TIME vs. DRAIN CURRENT



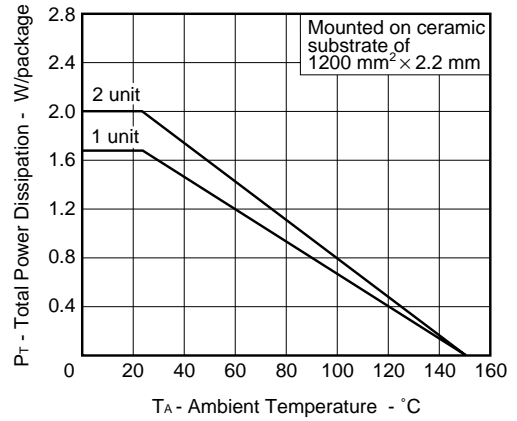
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



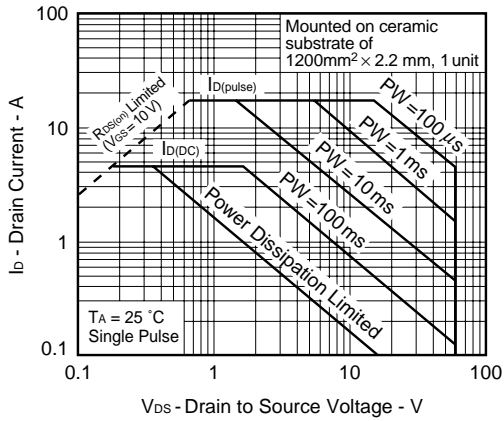
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



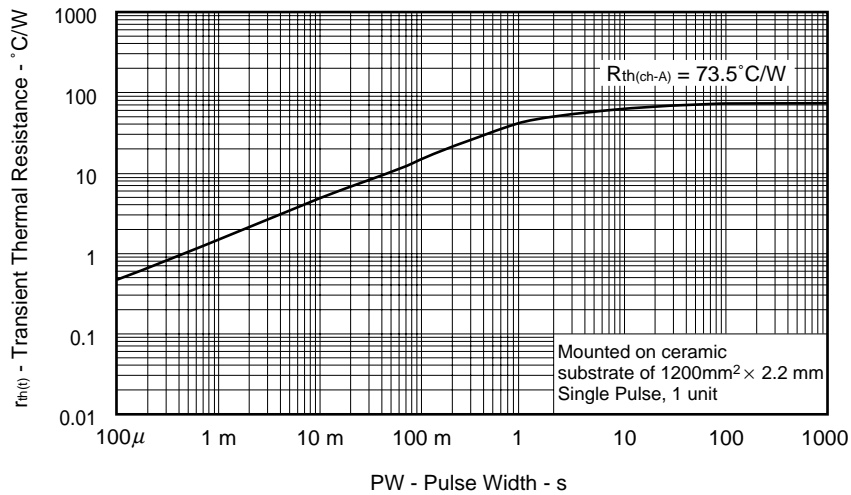
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

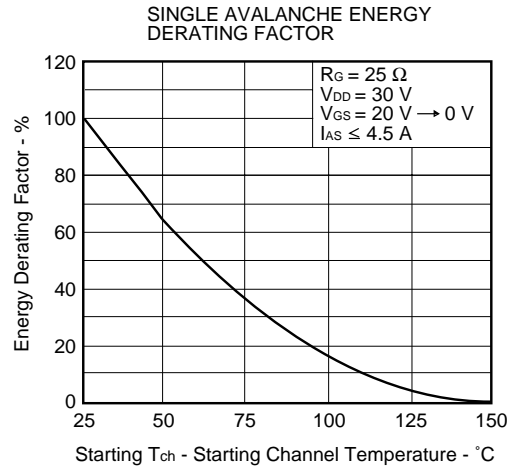
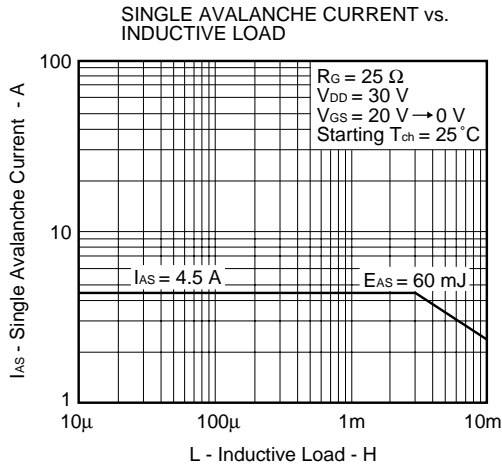


FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





[MEMO]

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