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April 1st, 2010
Renesas Electronics Corporation

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SWITCHING DUAL P-CHANNEL POWER MOS FET

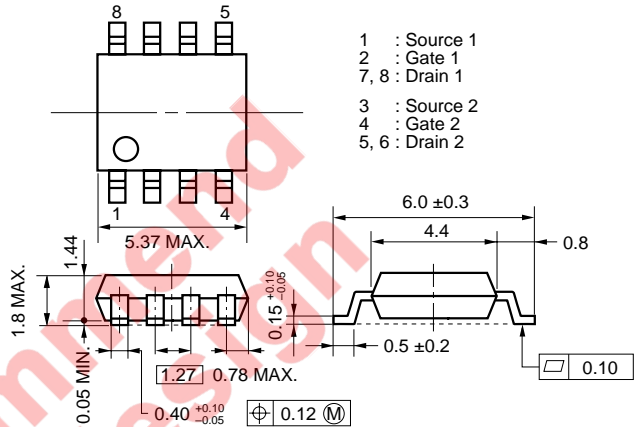
DESCRIPTION

The μPA1774 is Dual P-channel MOS Field Effect Transistor.

FEATURES

- Dual chip type
- Low on-state resistance
 $R_{DS(on)1} = 250 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -2.0 \text{ A)}$
 $R_{DS(on)2} = 300 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -2.0 \text{ A)}$
 $R_{DS(on)3} = 330 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.0 \text{ V, } I_D = -2.0 \text{ A)}$
- Low input capacitance
 $C_{iss} = 420 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



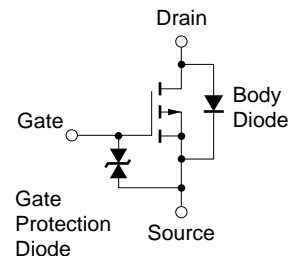
ORDERING INFORMATION

| PART NUMBER | PACKAGE |
|-------------|------------|
| μPA1774G | Power SOP8 |

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

| | | | |
|---|-----------------------|------------|----|
| Drain to Source Voltage (V _{GS} = 0 V) | V _{DSS} | -60 | V |
| Gate to Source Voltage (V _{DS} = 0 V) | V _{GSS} | ±20 | V |
| Drain Current (DC) (T _c = 25°C) | I _{D(DC)} | ±2.8 | A |
| Drain Current (pulse) ^{Note1} | I _{D(pulse)} | ±18 | A |
| Total Power Dissipation (1 unit) ^{Note2} | P _T | 0.6 | W |
| Total Power Dissipation (2 unit) ^{Note2} | P _T | 0.8 | W |
| Channel Temperature | T _{ch} | 150 | °C |
| Storage Temperature | T _{stg} | -55 to 150 | °C |
| Single Avalanche Current ^{Note3} | I _{AS} | -2.8 | A |
| Single Avalanche Energy ^{Note3} | E _{AS} | 0.78 | mJ |

EQUIVALENT CIRCUIT (1/2 circuit)



Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Mounted on Glass Epoxy Board of 1600 mm² x 1.6 mm. Drain pad size: 264 mm² x 35 μm, T_A = 25°C

3. Starting T_{ch} = 25°C, V_{DD} = -30 V, R_G = 25 Ω, V_{GS} = -20 → 0 V

Remark

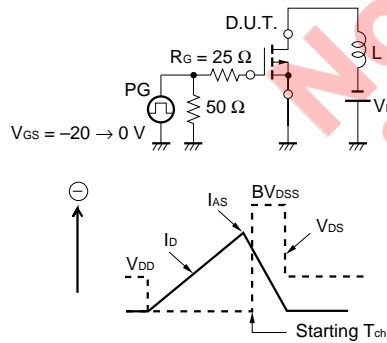
The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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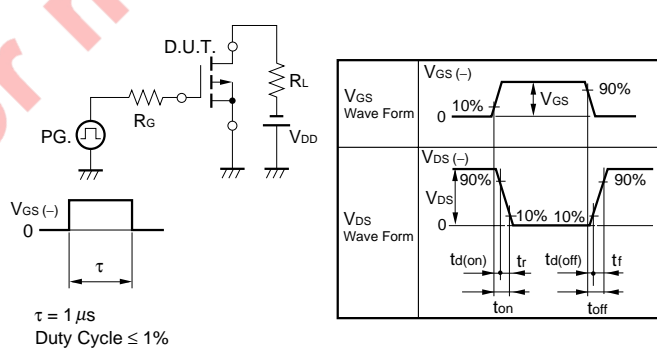
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|----------------------|---|------|------|------|------|
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = -60 V, V _{GS} = 0 V | | | -10 | μA |
| Gate Leakage Current | I _{GSS} | V _{GS} = ±16 V, V _{DS} = 0 V | | | ±10 | μA |
| Gate Cut-off Voltage | V _{GS(off)} | V _{DS} = -10 V, I _D = 1 mA | -1.5 | -2.0 | -2.5 | V |
| Forward Transfer Admittance | y _{fs} | V _{DS} = -10 V, I _D = -2.0 A | 2.5 | 4.3 | | S |
| Drain to Source On-state Resistance | R _{DS(on)1} | V _{GS} = -10 V, I _D = -2.0 A | | 200 | 250 | mΩ |
| | R _{DS(on)2} | V _{GS} = -4.5 V, I _D = -2.0 A | | 230 | 300 | mΩ |
| | R _{DS(on)3} | V _{GS} = -4.0 V, I _D = -2.0 A | | 240 | 330 | mΩ |
| Input Capacitance | C _{iss} | V _{DS} = -10 V | | 420 | | pF |
| Output Capacitance | C _{oss} | V _{GS} = 0 V | | 80 | | pF |
| Reverse Transfer Capacitance | C _{rss} | f = 1 MHz | | 30 | | pF |
| Turn-on Delay Time | t _{d(on)} | V _{DD} = -30 V, I _D = -2.0 A | | 8 | | ns |
| Rise Time | t _r | V _{GS} = -10 V | | 5 | | ns |
| Turn-off Delay Time | t _{d(off)} | R _G = 0 Ω | | 35 | | ns |
| Fall Time | t _f | | | 8 | | ns |
| Total Gate Charge | Q _G | V _{DD} = -48 V | | 10 | | nC |
| Gate to Source Charge | Q _{GS} | V _{GS} = -10 V | | 1.7 | | nC |
| Gate to Drain Charge | Q _{GD} | I _D = -2.8 A | | 2.2 | | nC |
| Body Diode Forward Voltage | V _{F(S-D)} | I _F = 2.8 A, V _{GS} = 0 V | | 0.89 | | V |
| Reverse Recovery Time | t _{rr} | I _F = 2.8 A, V _{GS} = 0 V | | 45 | | ns |
| Reverse Recovery Charge | Q _{rr} | di/dt = 100 A/μs | | 65 | | μC |

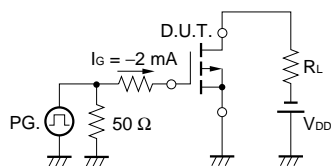
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

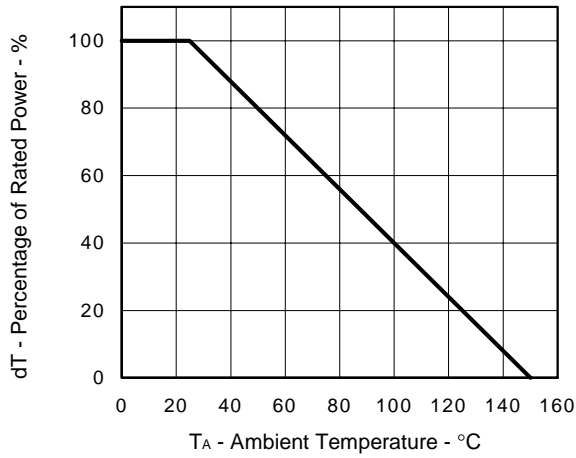


TEST CIRCUIT 3 GATE CHARGE

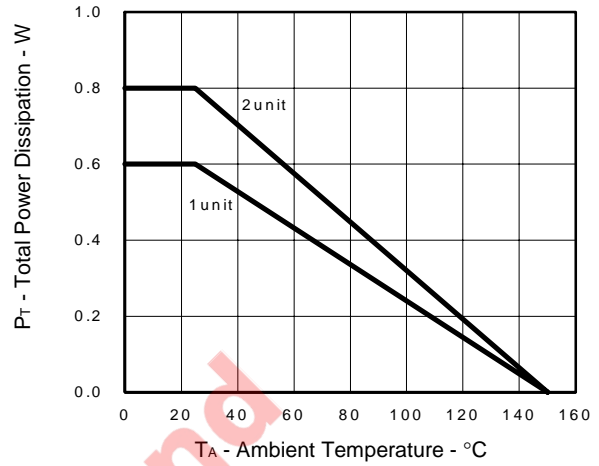


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

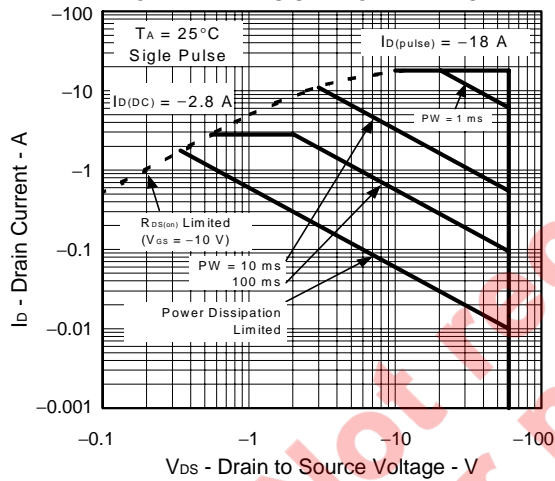
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



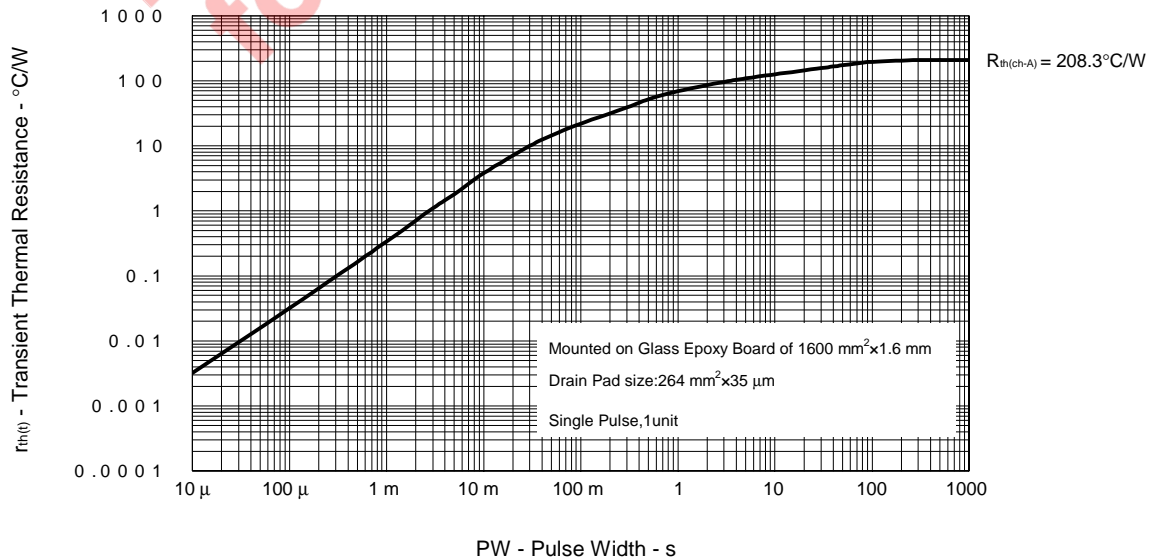
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

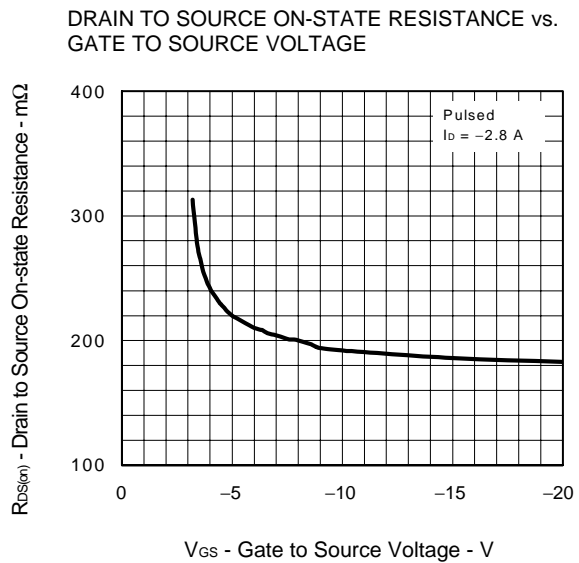
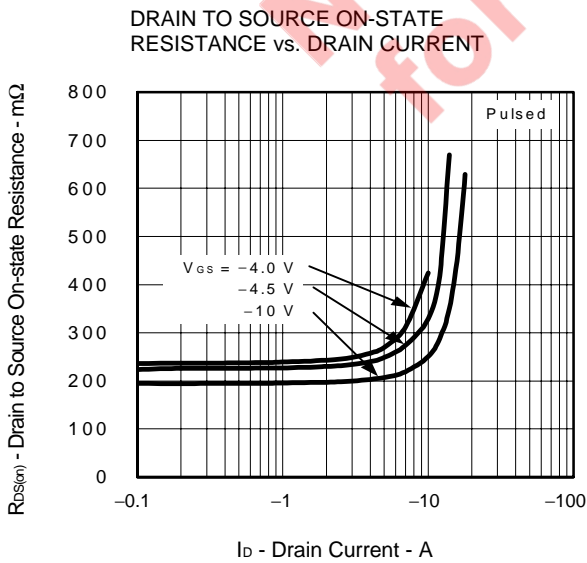
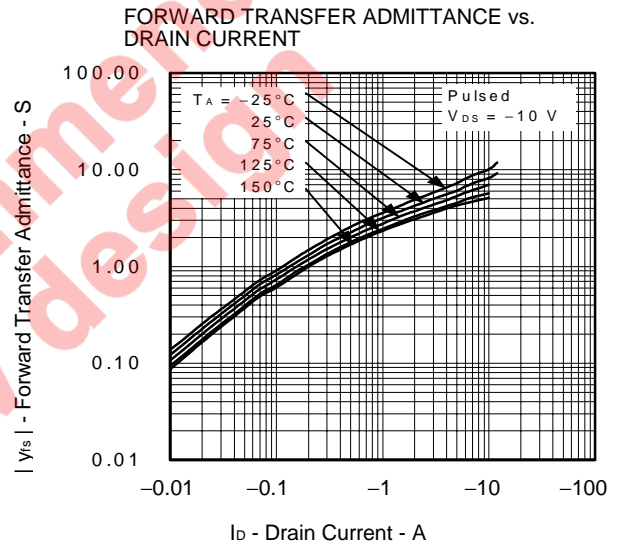
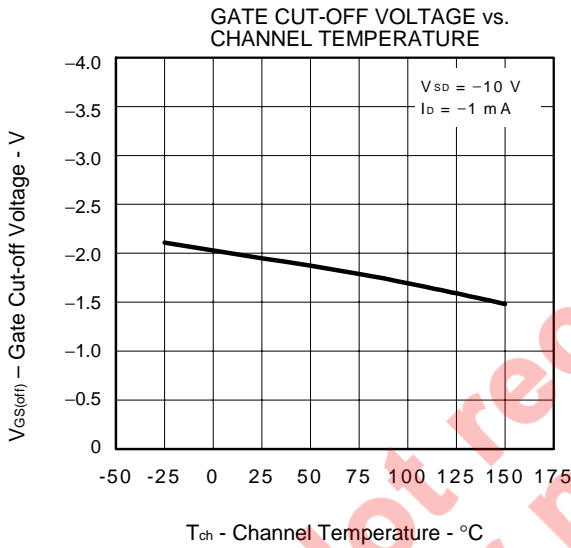
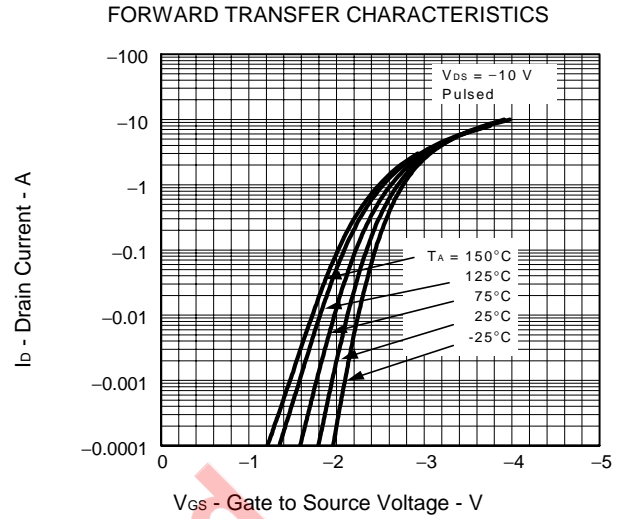
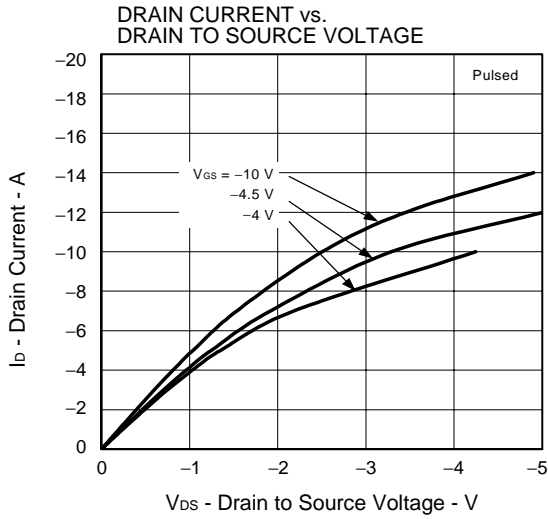


FORWARD BIAS SAFE OPERATING AREA

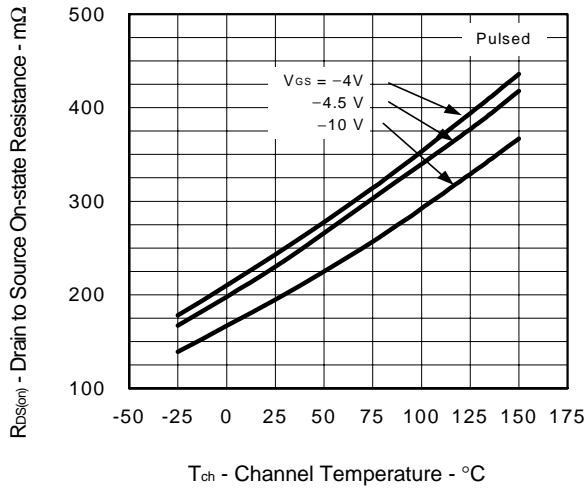


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

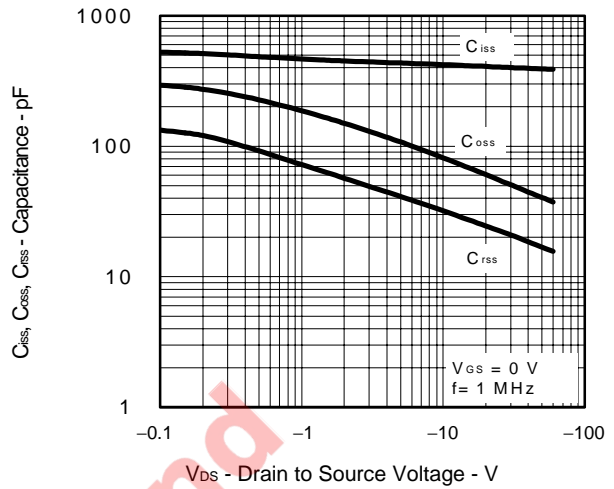




DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



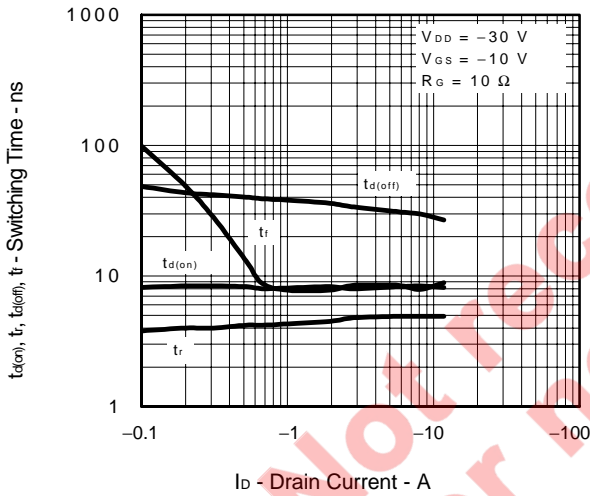
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



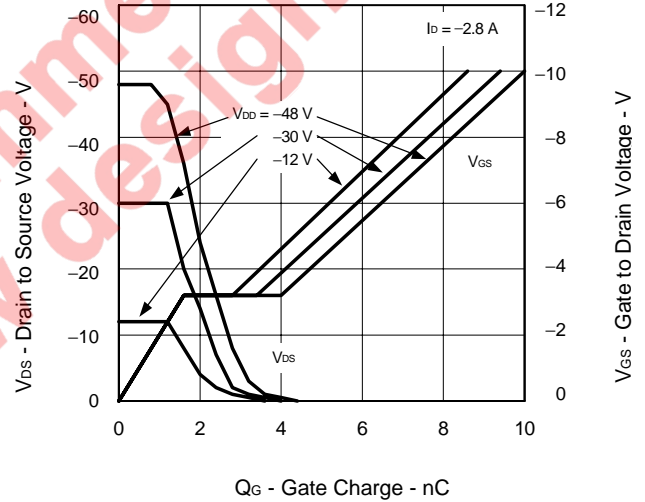
T_{ch} - Channel Temperature - $^{\circ}C$

V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS



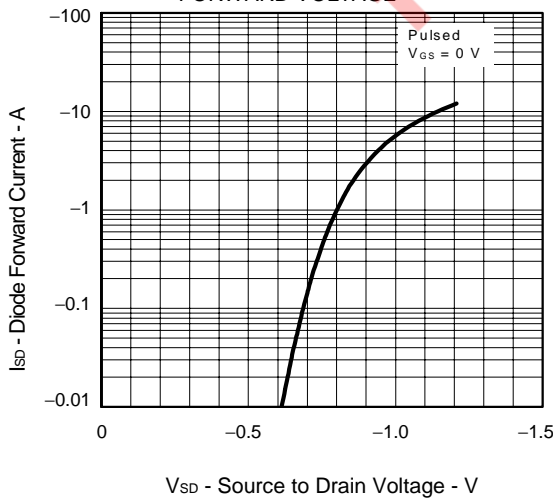
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



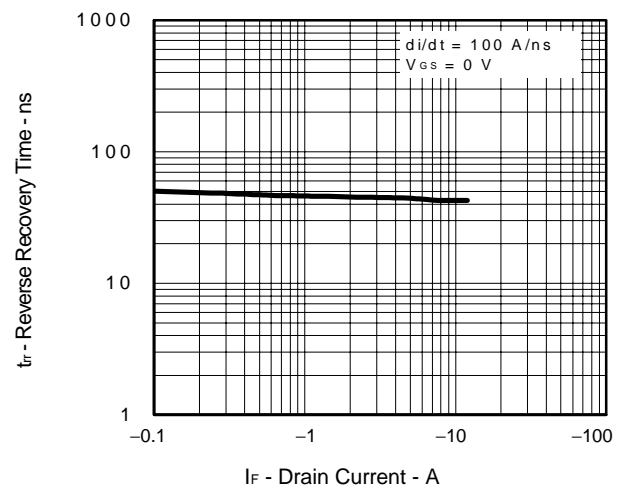
I_D - Drain Current - A

Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



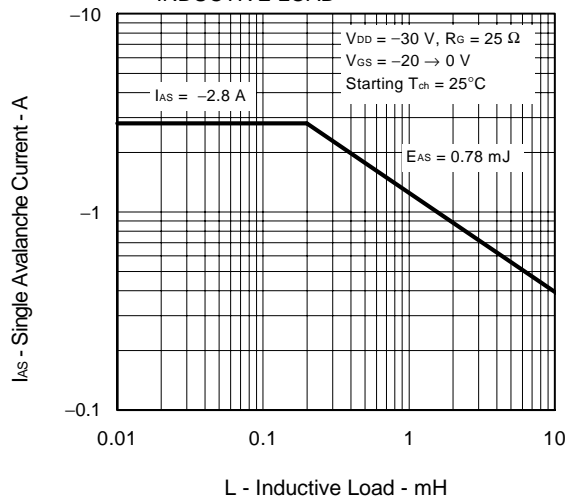
REVERSE RECOVERY TIME vs. DRAIN CURRENT



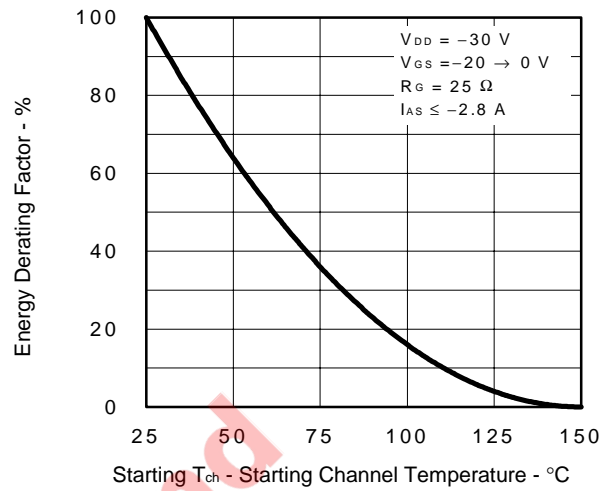
V_{SD} - Source to Drain Voltage - V

I_F - Drain Current - A

SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



Not recommended for new design

[MEMO]

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